

ZZZ1  
PCB

PJP1  
14W\_DCIN  
14W\_45@

PJP1  
15W\_DCIN  
15W\_45@

12/21 Add PJP1 for DCIN Cable on 45 Level  
One for 14W DCIN , PN: DC301001Y00  
Another for 15W DCIN , PN: DC301001V00

# Compal Confidential

## IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M  
(With nVIDIA MXM/B)

2006-1-31

REV: 0.3

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File Name : LA-3541P

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IDSEL:AD20  
(PIRQC#,PIRQD#,  
GNT#2, REQ#2)

IDSEL:AD22  
(PIRQG#,PIRQH#,  
GNT#0, REQ#0)

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS ( Actual +0.9V )	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## PROJECT ID Table

	ID1	ID0
IFT00 (00@)	R284	R283
IFT01 (01@)	R284	R281
IFL90 (10@)	R694	R283
IFT91 (11@)	R694	R281

## BOARD ID Table

R	Structure
Ra (R743)	15W@
Rb (R740)	14W@

## MIC ID Table

R	Structure
R785 Single MIC	INT@
R786 Array MIC	DUAL@

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

## EC SM Bus2 address

## ICH8M SM Bus address

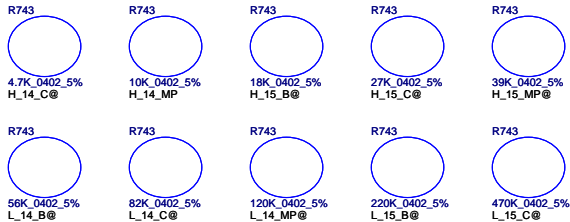
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

## SKU ID Table

Vcc	3.3V +/- 5%
Rb	47K +/- 5%

Rb~ R740

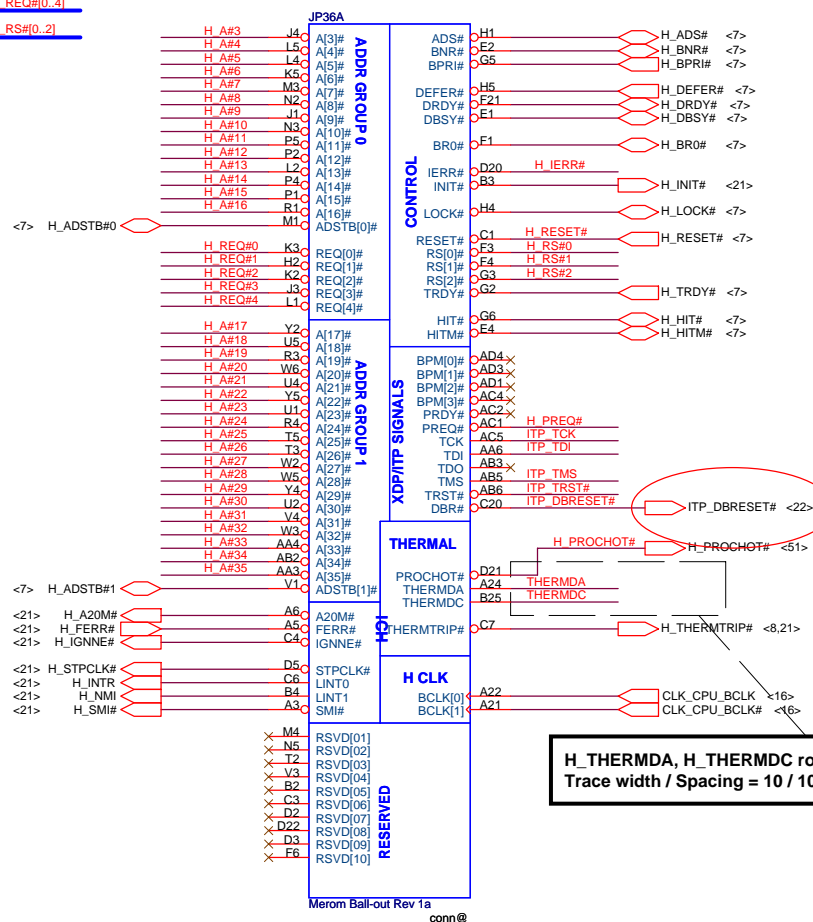
Ra~ R743



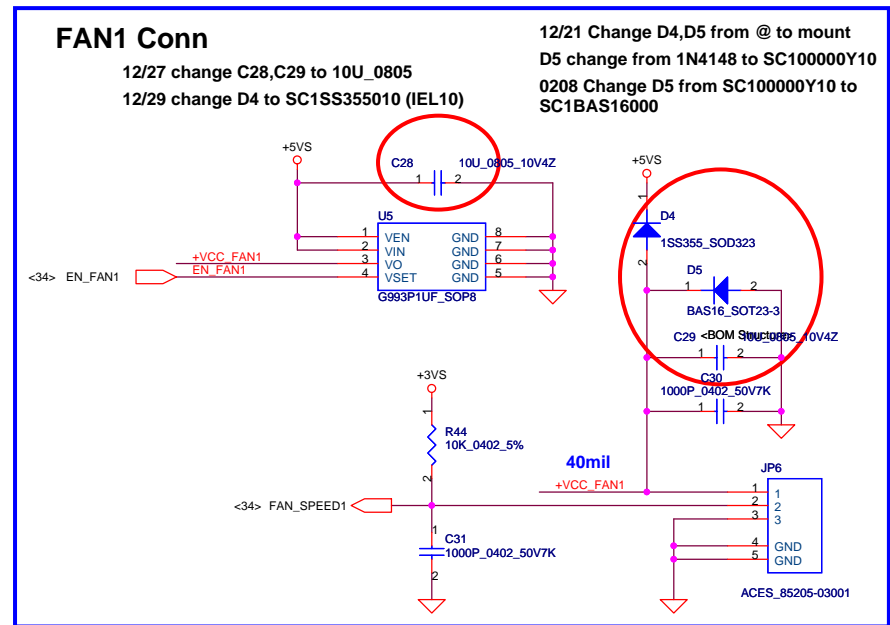
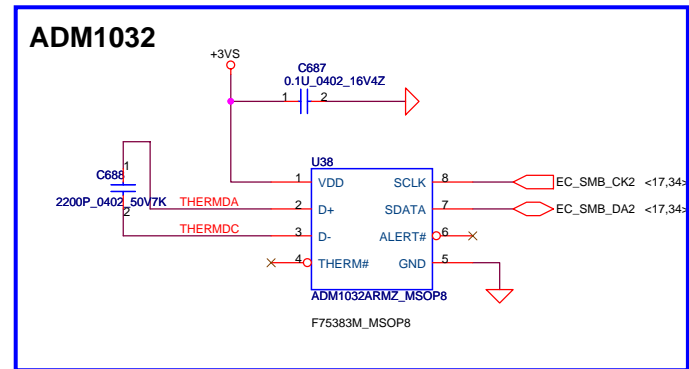
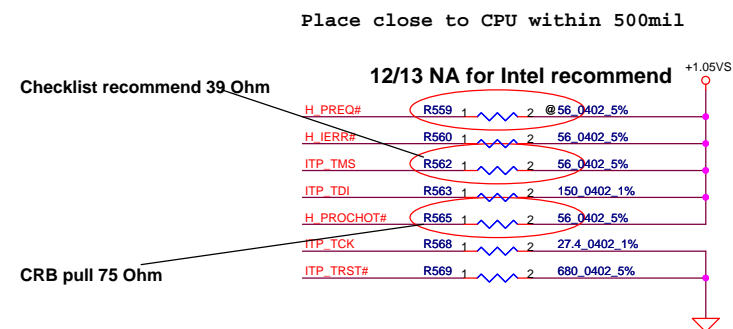
Board ID	Rb	Ra	VAD_BID min	VAD_BID typ	VAD_BID max	Ra BOM Structure
1	NA	4.7K +/- 5%	0 V	0 V	0 V	H_14_B@
2	47K(RB@)	4.7K +/- 5%	0.274 V	0.300 V	0.328 V	H_14_C@ ✓
3	47K(RB@)	10K +/- 5%	0.553V	0.578 V	0.628 V	H_14_MP@
4	47K(RB@)	18K +/- 5%	0.849V	0.913V	0.981 V	H_15_B@
5	47K(RB@)	27K +/- 5%	1.129 V	1.204 V	1.282 V	H_15_C@ ✓
6	47K(RB@)	39K +/- 5%	1.415 V	1.496 V	1.579 V	H_15_MP@
7	47K(RB@)	56K +/- 5%	1.712 V	1.794 V	1.876 V	L_14_B@
8	47K(RB@)	82K +/- 5%	2.020V	2.097 V	2.173 V	L_14_C@ ✓
9	47K(RB@)	120K +/- 5%	2.303 V	2.371 V	2.437 V	L_14_MP@
10	47K(RB@)	220K +/- 5%	2.670 V	2.719 V	2.765 V	L_15_B@
11	47K(RB@)	470K +/- 5%	2.972 V	3.000 V	3.026 V	L_15_C@ ✓
12	47K(RB@)	NA	3.135 V	3.300 V	3.465 V	NA for L_15_MP

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<7> H\_A#[3..35] H\_A#[3..35]  
 <7> H\_REQ#[0..4] H\_REQ#[0..4]  
 <7> H\_RS#[0..2] H\_RS#[0..2]

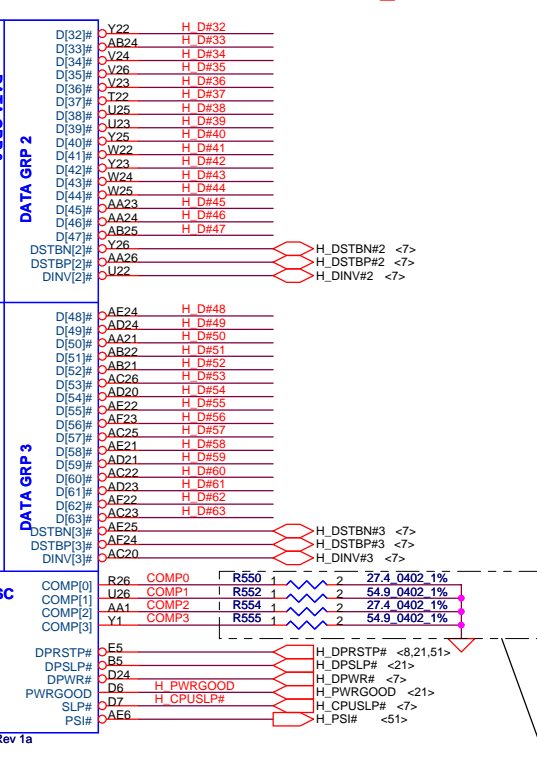
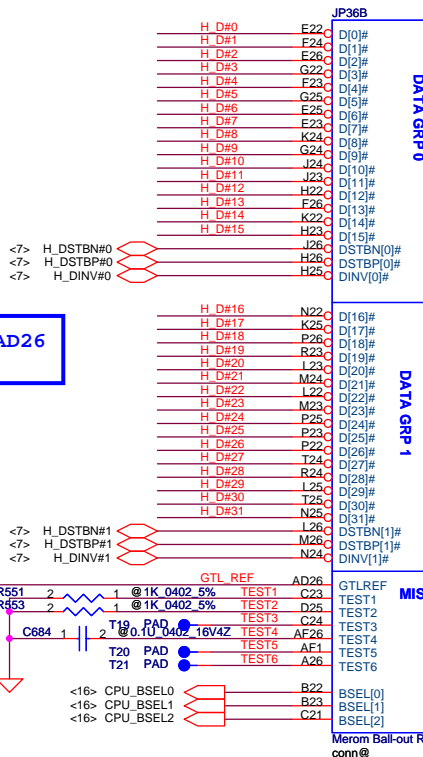
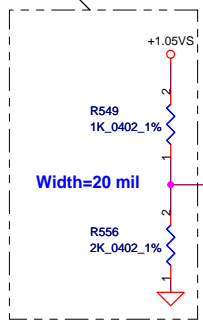


H\_THERMDA, H\_THERMDC routing together,  
 Trace width / Spacing = 10 / 10 mil



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								Merom (1/3)									
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Close to CPU pin AD26  
within 500mils.



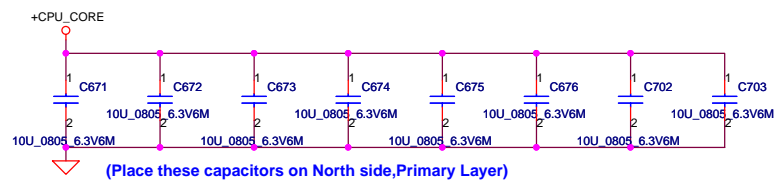
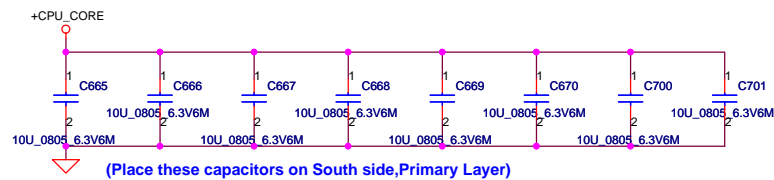
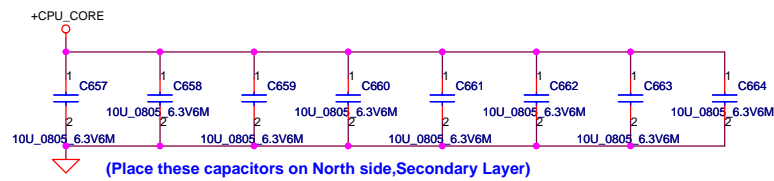
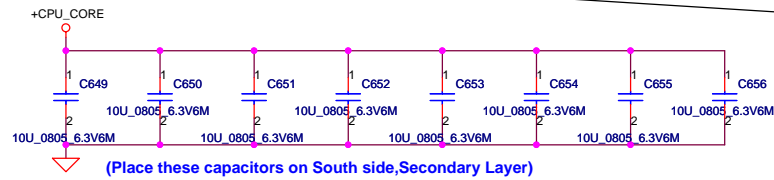
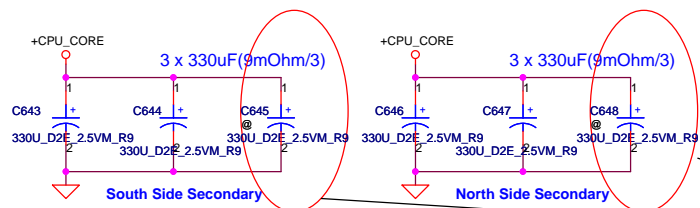
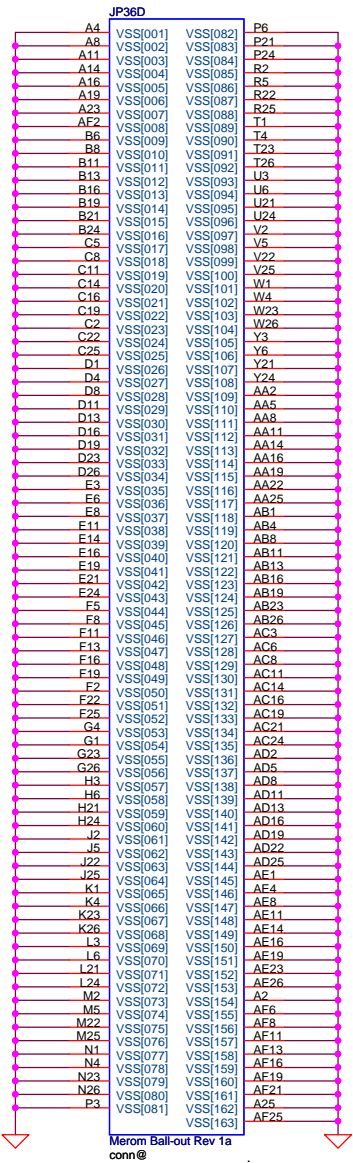
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

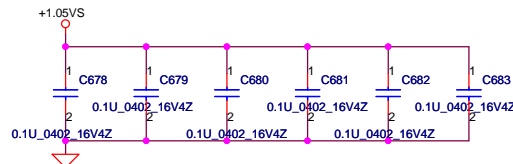
Resistor placed within  
0.5" of CPU pin. Trace  
should be at least 25  
mils away from any other  
toggling signal.  
COMP[0,2] trace width is  
18 mils. COMP[1,3] trace  
width is 4 mils.

Length match within 25 mils.  
The trace width/space/other is  
20/7/25.

Close to CPU pin  
within 500mils.



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

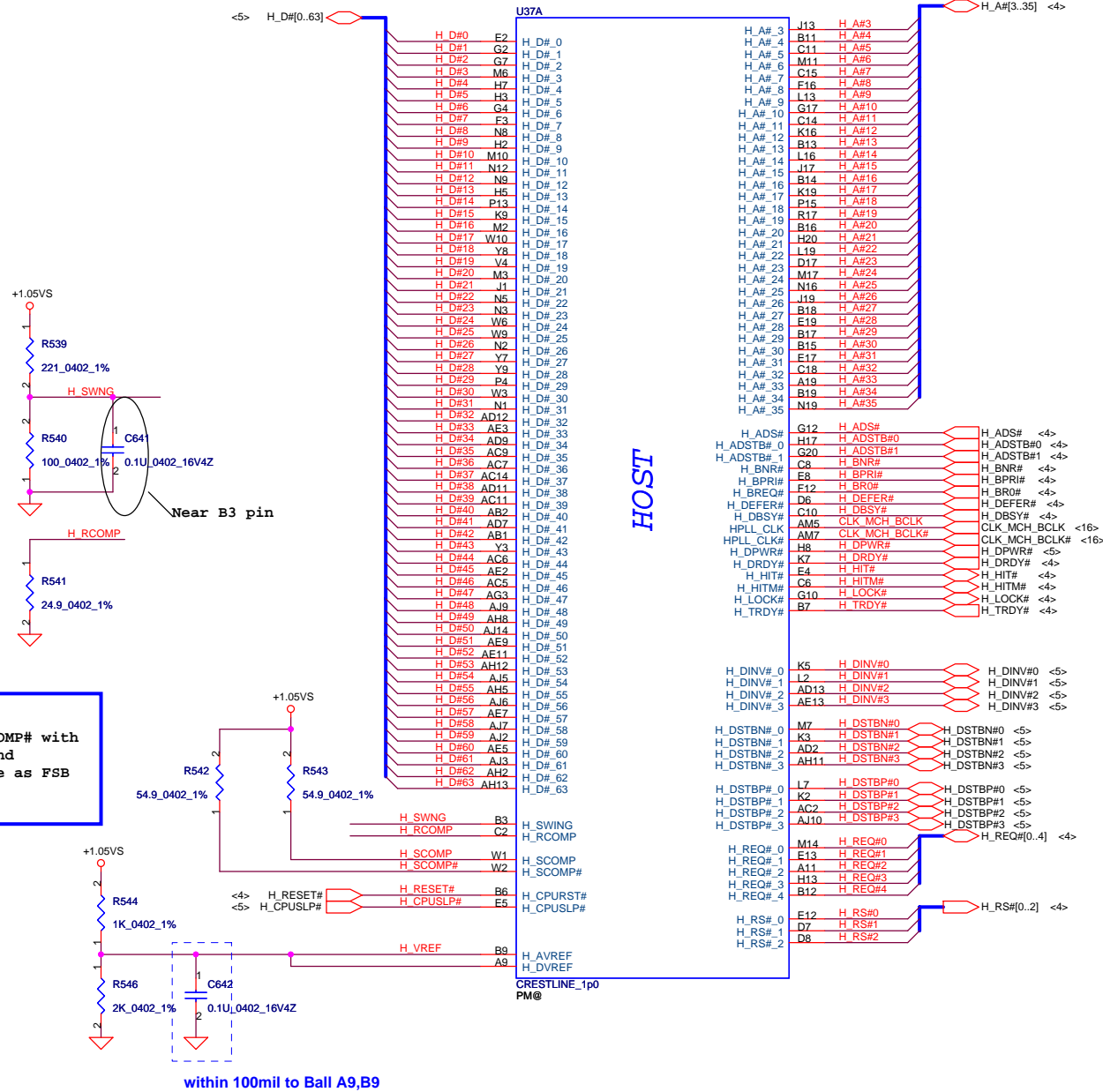


CRB no stuff. Reserved!

9/25 10U checked. OK for use!

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1/2 change U37 PM part number to SA00001DJ90

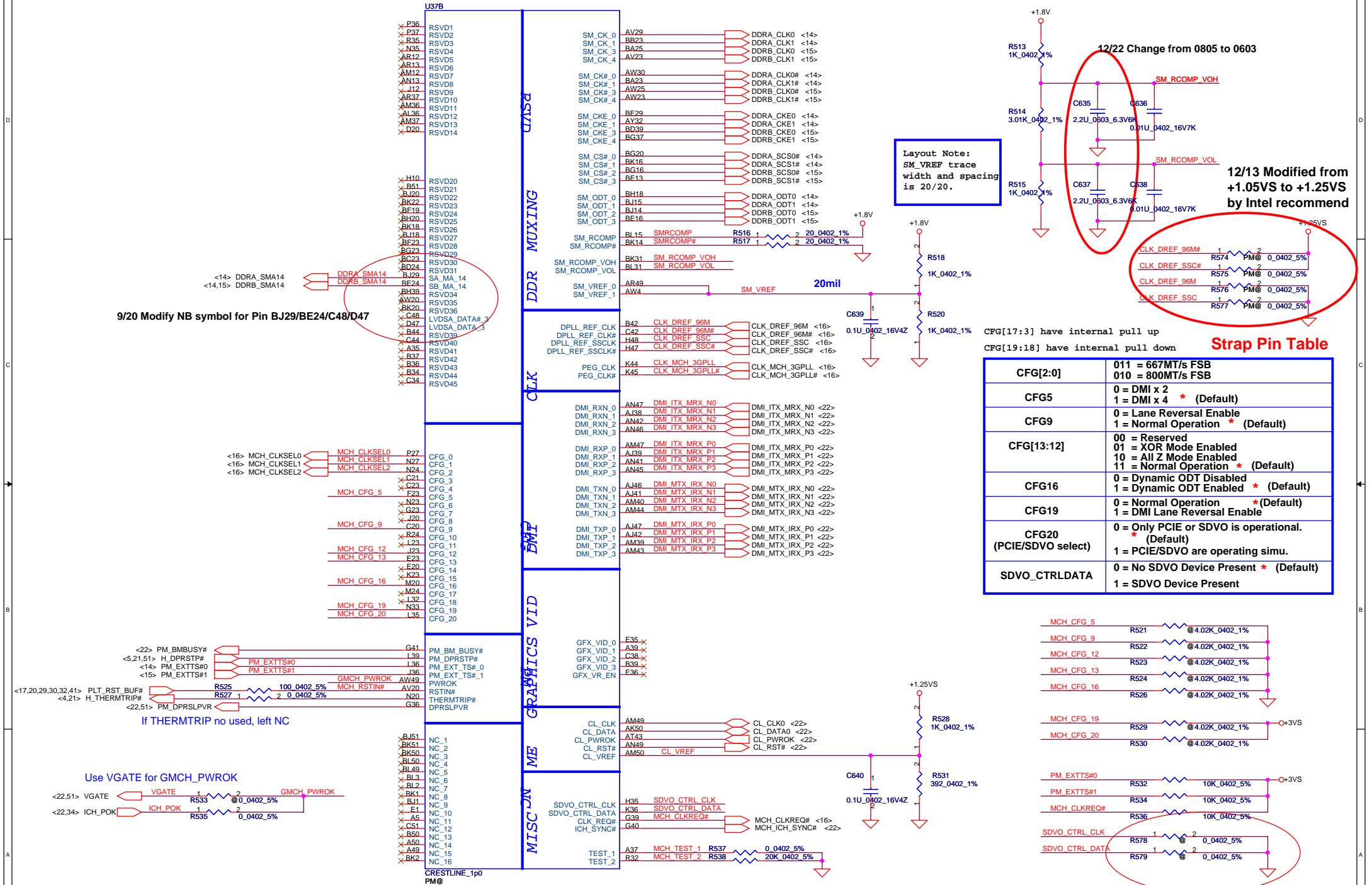


1/2 change U37 GM part number to SA00000ZW80

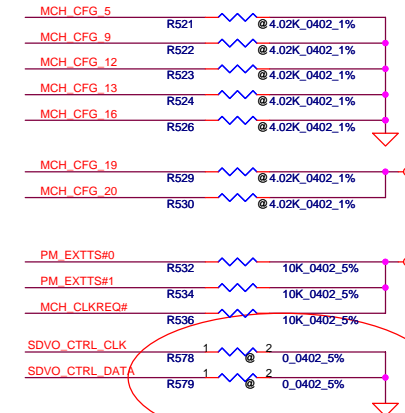
Layout Note:  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

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								Crestline (1/7)-GTL						
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Strap Pin Table	
CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simul.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present





<14> DDRA\_SDQ[0..63] <14> DDRA\_SDM[0..7] <14> DDRA\_SMA[0..13]

<15> DDRB\_SDQ[0..63] <15> DDRB\_SDM[0..7] <15> DDRB\_SMA[0..13]

U37D  
DDRA\_SDQ0 AR43 SA\_DQ\_0  
DDRA\_SDQ1 AW44 SA\_DQ\_1  
DDRA\_SDQ2 BA45 SA\_DQ\_2  
DDRA\_SDQ3 AY46 SA\_DQ\_3  
DDRA\_SDQ4 AR41 SA\_DQ\_4  
DDRA\_SDQ5 AR45 SA\_DQ\_5  
DDRA\_SDQ6 AT42 SA\_DQ\_6  
DDRA\_SDQ7 AW47 SA\_DQ\_7  
DDRA\_SDQ8 BB45 SA\_DQ\_8  
DDRA\_SDQ9 BF48 SA\_DQ\_9  
DDRA\_SDQ10 BG47 SA\_DQ\_10  
DDRA\_SDQ11 BA45 SA\_DQ\_11  
DDRA\_SDQ12 BB47 SA\_DQ\_12  
DDRA\_SDQ13 BG50 SA\_DQ\_13  
DDRA\_SDQ14 BH49 SA\_DQ\_14  
DDRA\_SDQ15 BE45 SA\_DQ\_15  
DDRA\_SDQ16 AW43 SA\_DQ\_16  
DDRA\_SDQ17 BA44 SA\_DQ\_17  
DDRA\_SDQ18 BG42 SA\_DQ\_18  
DDRA\_SDQ19 BE40 SA\_DQ\_19  
DDRA\_SDQ20 BF44 SA\_DQ\_20  
DDRA\_SDQ21 BH45 SA\_DQ\_21  
DDRA\_SDQ22 BG40 SA\_DQ\_22  
DDRA\_SDQ23 BE40 SA\_DQ\_23  
DDRA\_SDQ24 AR40 SA\_DQ\_24  
DDRA\_SDQ25 AW40 SA\_DQ\_25  
DDRA\_SDQ26 AT39 SA\_DQ\_26  
DDRA\_SDQ27 AW36 SA\_DQ\_27  
DDRA\_SDQ28 AW41 SA\_DQ\_28  
DDRA\_SDQ29 AY41 SA\_DQ\_29  
DDRA\_SDQ30 AV38 SA\_DQ\_30  
DDRA\_SDQ31 AT38 SA\_DQ\_31  
DDRA\_SDQ32 AV13 SA\_DQ\_32  
DDRA\_SDQ33 AT13 SA\_DQ\_33  
DDRA\_SDQ34 AW11 SA\_DQ\_34  
DDRA\_SDQ35 AV11 SA\_DQ\_35  
DDRA\_SDQ36 AU15 SA\_DQ\_36  
DDRA\_SDQ37 AT11 SA\_DQ\_37  
DDRA\_SDQ38 BA13 SA\_DQ\_38  
DDRA\_SDQ39 BA11 SA\_DQ\_39  
DDRA\_SDQ40 BE10 SA\_DQ\_40  
DDRA\_SDQ41 BD10 SA\_DQ\_41  
DDRA\_SDQ42 BD8 SA\_DQ\_42  
DDRA\_SDQ43 AY9 SA\_DQ\_43  
DDRA\_SDQ44 BG10 SA\_DQ\_44  
DDRA\_SDQ45 AW9 SA\_DQ\_45  
DDRA\_SDQ46 BD7 SA\_DQ\_46  
DDRA\_SDQ47 BB9 SA\_DQ\_47  
DDRA\_SDQ48 BB5 SA\_DQ\_48  
DDRA\_SDQ49 AY7 SA\_DQ\_49  
DDRA\_SDQ50 AT5 SA\_DQ\_50  
DDRA\_SDQ51 AT7 SA\_DQ\_51  
DDRA\_SDQ52 AY6 SA\_DQ\_52  
DDRA\_SDQ53 BB7 SA\_DQ\_53  
DDRA\_SDQ54 AR5 SA\_DQ\_54  
DDRA\_SDQ55 AR8 SA\_DQ\_55  
DDRA\_SDQ56 AR9 SA\_DQ\_56  
DDRA\_SDQ57 AN3 SA\_DQ\_57  
DDRA\_SDQ58 AN8 SA\_DQ\_58  
DDRA\_SDQ59 AN10 SA\_DQ\_59  
DDRA\_SDQ60 AT9 SA\_DQ\_60  
DDRA\_SDQ61 AN9 SA\_DQ\_61  
DDRA\_SDQ62 AM9 SA\_DQ\_62  
DDRA\_SDQ63 AN11 SA\_DQ\_63

CRESTLINE\_1p0  
PM@

DDR SYSTEM MEMORY A

SA\_BS\_0 BB19 <14>  
SA\_BS\_1 BK19 <14>  
SA\_BS\_2 BF29 <14>  
SA\_CAS# BL17 <14>  
SA\_DM\_0 AT45 DDRA\_SDM0  
SA\_DM\_1 BD44 DDRA\_SDM1  
SA\_DM\_2 BD42 DDRA\_SDM2  
SA\_DM\_3 AW38 DDRA\_SDM3  
SA\_DM\_4 AW13 DDRA\_SDM4  
SA\_DM\_5 BG8 DDRA\_SDM5  
SA\_DM\_6 AV5 DDRA\_SDM6  
SA\_DM\_7 AN6 DDRA\_SDM7  
SA\_DQS\_0 AT46 DDRA\_SQDS0 <14>  
SA\_DQS\_1 BE48 DDRA\_SQDS1 <14>  
SA\_DQS\_2 BB43 DDRA\_SQDS2 <14>  
SA\_DQS\_3 BC37 DDRA\_SQDS3 <14>  
SA\_DQS\_4 BB16 DDRA\_SQDS4 <14>  
SA\_DQS\_5 BH6 DDRA\_SQDS5 <14>  
SA\_DQS\_6 BB2 DDRA\_SQDS6 <14>  
SA\_DQS\_7 AP3 DDRA\_SQDS7 <14>  
SA\_DQS#\_0 AT47 DDRA\_SQDS0# <14>  
SA\_DQS#\_1 BD47 DDRA\_SQDS1# <14>  
SA\_DQS#\_2 BC41 DDRA\_SQDS2# <14>  
SA\_DQS#\_3 BA37 DDRA\_SQDS3# <14>  
SA\_DQS#\_4 BA16 DDRA\_SQDS4# <14>  
SA\_DQS#\_5 BH7 DDRA\_SQDS5# <14>  
SA\_DQS#\_6 BC1 DDRA\_SQDS6# <14>  
SA\_DQS#\_7 AP2 DDRA\_SQDS7# <14>  
SA\_MA\_0 BJ19 DDRA\_SMA0  
SA\_MA\_1 BD20 DDRA\_SMA1  
SA\_MA\_2 BK27 DDRA\_SMA2  
SA\_MA\_3 BH28 DDRA\_SMA3  
SA\_MA\_4 BL24 DDRA\_SMA4  
SA\_MA\_5 BK28 DDRA\_SMA5  
SA\_MA\_6 BJ27 DDRA\_SMA6  
SA\_MA\_7 BJ25 DDRA\_SMA7  
SA\_MA\_8 BL28 DDRA\_SMA8  
SA\_MA\_9 BA28 DDRA\_SMA9  
SA\_MA\_10 BC19 DDRA\_SMA10  
SA\_MA\_11 BE28 DDRA\_SMA11  
SA\_MA\_12 BG30 DDRA\_SMA12  
SA\_MA\_13 BJ16 DDRA\_SMA13  
SA\_RAS# BE18 <14>  
SA\_RCVEN# AY20 SA\_RCVEN# <14>  
SA\_WE# BA19 <14>

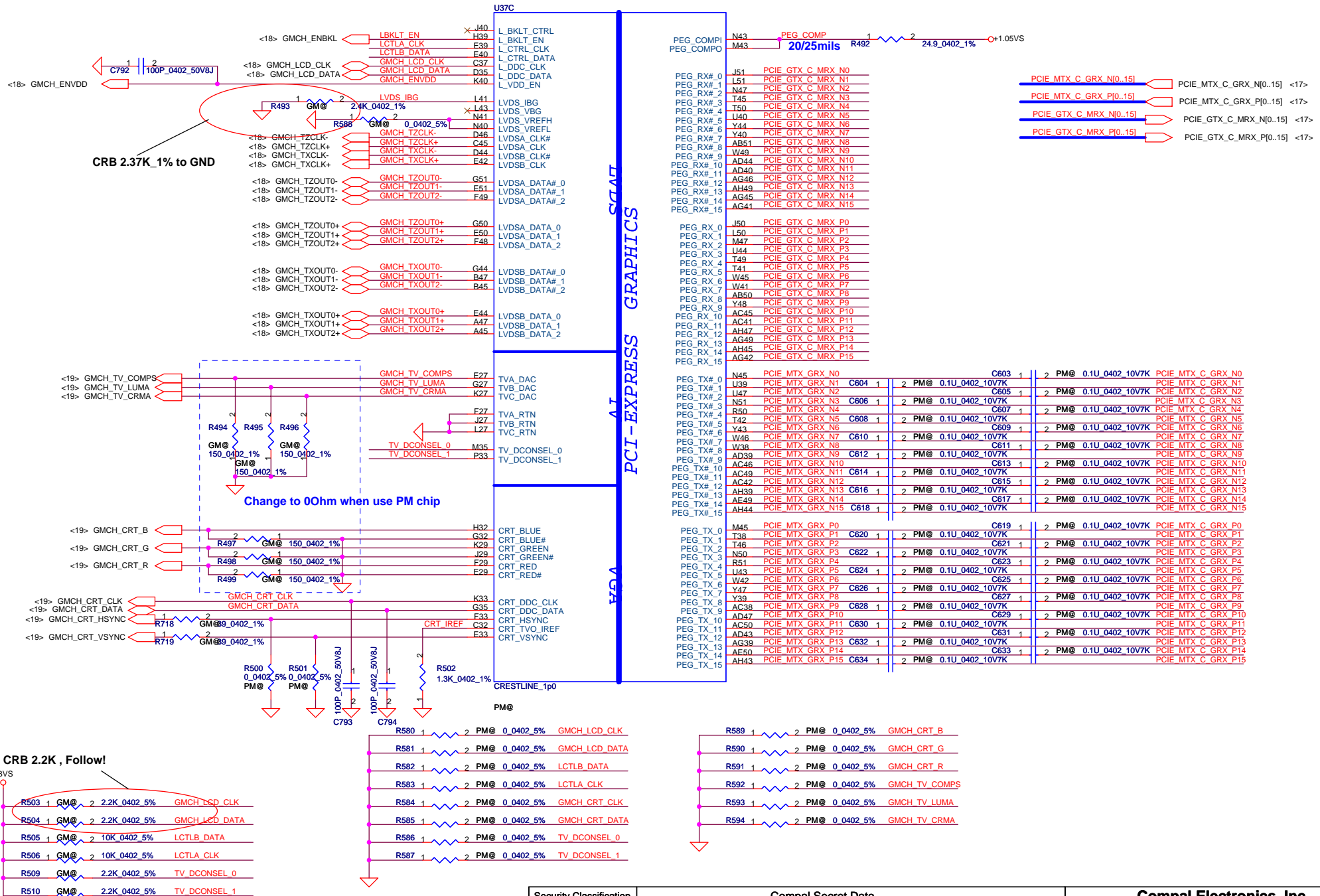
U37E  
DDRBDQ0 AP49 SB\_DQ\_0  
DDRBDQ1 AR51 SB\_DQ\_1  
DDRBDQ2 AW50 SB\_DQ\_2  
DDRBDQ3 AW51 SB\_DQ\_3  
DDRBDQ4 AN51 SB\_DQ\_4  
DDRBDQ5 AN50 SB\_DQ\_5  
DDRBDQ6 AV50 SB\_DQ\_6  
DDRBDQ7 AV49 SB\_DQ\_7  
DDRBDQ8 BA50 SB\_DQ\_8  
DDRBDQ9 BB50 SB\_DQ\_9  
DDRBDQ10 BA49 SB\_DQ\_10  
DDRBDQ11 BE50 SB\_DQ\_11  
DDRBDQ12 BA51 SB\_DQ\_12  
DDRBDQ13 AY49 SB\_DQ\_13  
DDRBDQ14 BF50 SB\_DQ\_14  
DDRBDQ15 BF49 SB\_DQ\_15  
DDRBDQ16 BJ50 SB\_DQ\_16  
DDRBDQ17 BJ44 SB\_DQ\_17  
DDRBDQ18 BJ43 SB\_DQ\_18  
DDRBDQ19 BL43 SB\_DQ\_19  
DDRBDQ20 BK47 SB\_DQ\_20  
DDRBDQ21 BK49 SB\_DQ\_21  
DDRBDQ22 BK43 SB\_DQ\_22  
DDRBDQ23 BK42 SB\_DQ\_23  
DDRBDQ24 BJ41 SB\_DQ\_24  
DDRBDQ25 BL41 SB\_DQ\_25  
DDRBDQ26 BJ37 SB\_DQ\_26  
DDRBDQ27 BJ36 SB\_DQ\_27  
DDRBDQ28 BK41 SB\_DQ\_28  
DDRBDQ29 BJ40 SB\_DQ\_29  
DDRBDQ30 BL36 SB\_DQ\_30  
DDRBDQ31 BK37 SB\_DQ\_31  
DDRBDQ32 BK13 SB\_DQ\_32  
DDRBDQ33 BE11 SB\_DQ\_33  
DDRBDQ34 BK11 SB\_DQ\_34  
DDRBDQ35 BC11 SB\_DQ\_35  
DDRBDQ36 BC13 SB\_DQ\_36  
DDRBDQ37 BE12 SB\_DQ\_37  
DDRBDQ38 BC12 SB\_DQ\_38  
DDRBDQ39 BG12 SB\_DQ\_39  
DDRBDQ40 BJ10 SB\_DQ\_40  
DDRBDQ41 BL9 SB\_DQ\_41  
DDRBDQ42 BK5 SB\_DQ\_42  
DDRBDQ43 BL5 SB\_DQ\_43  
DDRBDQ44 BK9 SB\_DQ\_44  
DDRBDQ45 BK10 SB\_DQ\_45  
DDRBDQ46 BJ8 SB\_DQ\_46  
DDRBDQ47 BL6 SB\_DQ\_47  
DDRBDQ48 BF4 SB\_DQ\_48  
DDRBDQ49 BH5 SB\_DQ\_49  
DDRBDQ50 BG1 SB\_DQ\_50  
DDRBDQ51 BC2 SB\_DQ\_51  
DDRBDQ52 BK3 SB\_DQ\_52  
DDRBDQ53 BE4 SB\_DQ\_53  
DDRBDQ54 BD3 SB\_DQ\_54  
DDRBDQ55 BJ2 SB\_DQ\_55  
DDRBDQ56 BA3 SB\_DQ\_56  
DDRBDQ57 BB3 SB\_DQ\_57  
DDRBDQ58 AR1 SB\_DQ\_58  
DDRBDQ59 AT3 SB\_DQ\_59  
DDRBDQ60 AY2 SB\_DQ\_60  
DDRBDQ61 AY3 SB\_DQ\_61  
DDRBDQ62 AU2 SB\_DQ\_62  
DDRBDQ63 AT2 SB\_DQ\_63

DDR SYSTEM MEMORY B

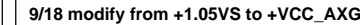
SB\_BS\_0 AY17 <15>  
SB\_BS\_1 BG18 <15>  
SB\_BS\_2 BG36 <15>  
SB\_CAS# BE17 <15>  
SB\_DM\_0 AR50 DDRB\_SDM0  
SB\_DM\_1 BD49 DDRB\_SDM1  
SB\_DM\_2 BK45 DDRB\_SDM2  
SB\_DM\_3 BL39 DDRB\_SDM3  
SB\_DM\_4 BH12 DDRB\_SDM4  
SB\_DM\_5 BJ7 DDRB\_SDM5  
SB\_DM\_6 BE3 DDRB\_SDM6  
SB\_DM\_7 AW2 DDRB\_SDM7  
SB\_DQS\_0 AT50 DDRB\_SQDS0 <15>  
SB\_DQS\_1 BD50 DDRB\_SQDS1 <15>  
SB\_DQS\_2 BK46 DDRB\_SQDS2 <15>  
SB\_DQS\_3 BK39 DDRB\_SQDS3 <15>  
SB\_DQS\_4 BJ12 DDRB\_SQDS4 <15>  
SB\_DQS\_5 BL7 DDRB\_SQDS5 <15>  
SB\_DQS\_6 BE2 DDRB\_SQDS6 <15>  
SB\_DQS\_7 AV2 DDRB\_SQDS7 <15>  
SB\_DQS#\_0 AU50 DDRB\_SQDS0# <15>  
SB\_DQS#\_1 BC50 DDRB\_SQDS1# <15>  
SB\_DQS#\_2 BL45 DDRB\_SQDS2# <15>  
SB\_DQS#\_3 BK38 DDRB\_SQDS3# <15>  
SB\_DQS#\_4 BK12 DDRB\_SQDS4# <15>  
SB\_DQS#\_5 BK7 DDRB\_SQDS5# <15>  
SB\_DQS#\_6 BF2 DDRB\_SQDS6# <15>  
SB\_DQS#\_7 AV3 DDRB\_SQDS7# <15>  
SB\_MA\_0 BC18 DDRB\_SMA0  
SB\_MA\_1 BG28 DDRB\_SMA1  
SB\_MA\_2 BG25 DDRB\_SMA2  
SB\_MA\_3 AW17 DDRB\_SMA3  
SB\_MA\_4 BE25 DDRB\_SMA4  
SB\_MA\_5 BE25 DDRB\_SMA5  
SB\_MA\_6 BA29 DDRB\_SMA6  
SB\_MA\_7 BC28 DDRB\_SMA7  
SB\_MA\_8 AY28 DDRB\_SMA8  
SB\_MA\_9 BD37 DDRB\_SMA9  
SB\_MA\_10 BG17 DDRB\_SMA10  
SB\_MA\_11 BE37 DDRB\_SMA11  
SB\_MA\_12 BA39 DDRB\_SMA12  
SB\_MA\_13 BG13 DDRB\_SMA13  
SB\_RAS# AV16 <15>  
SB\_RCVEN# AY18 SB\_RCVEN# <15>  
SB\_WE# BC17 <15>

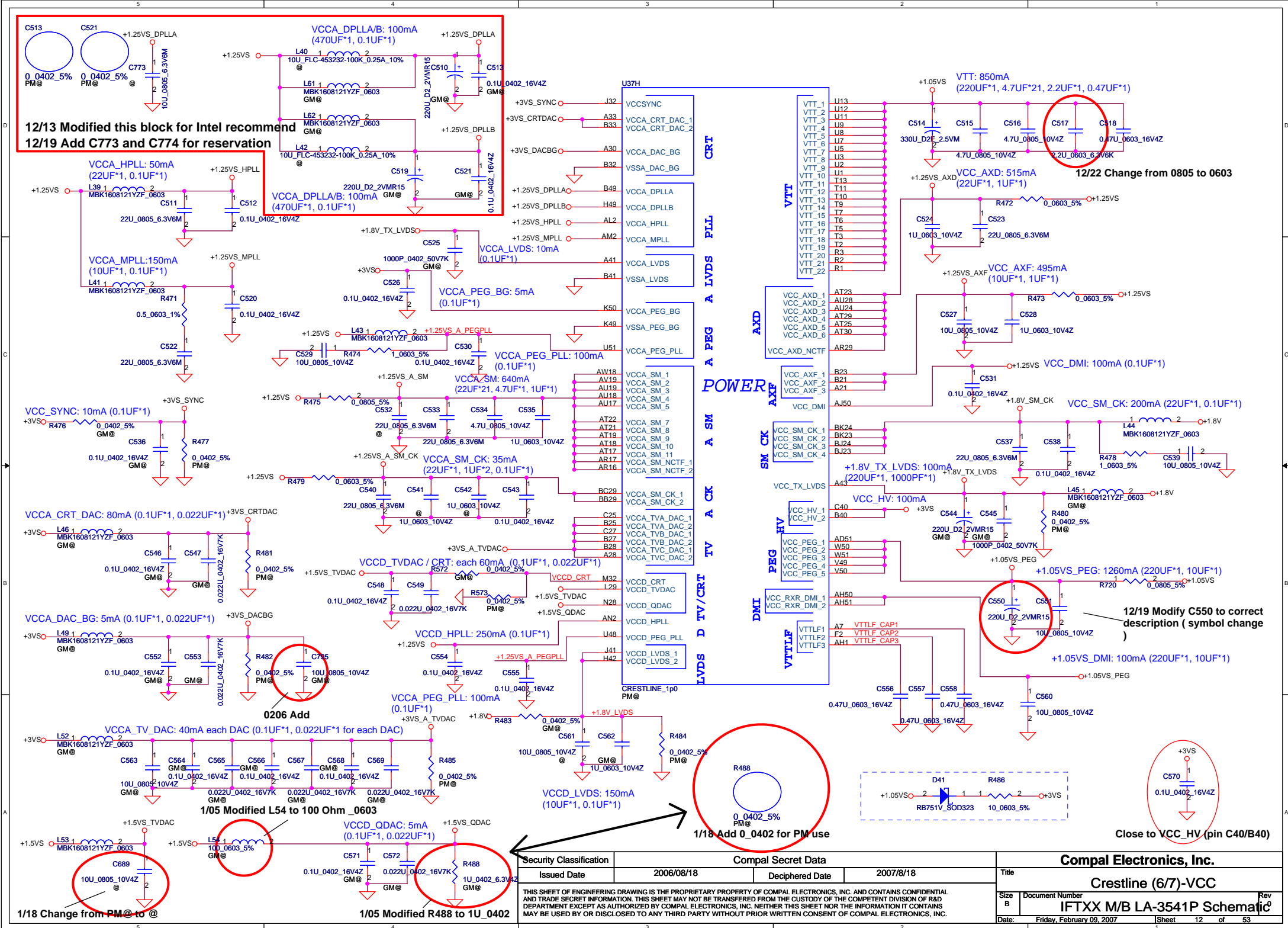
CRESTLINE\_1p0  
PM@

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Compal Electronics, Inc.	
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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev	0
Date:	Thursday, February 08, 2007	Sheet	9	of	53

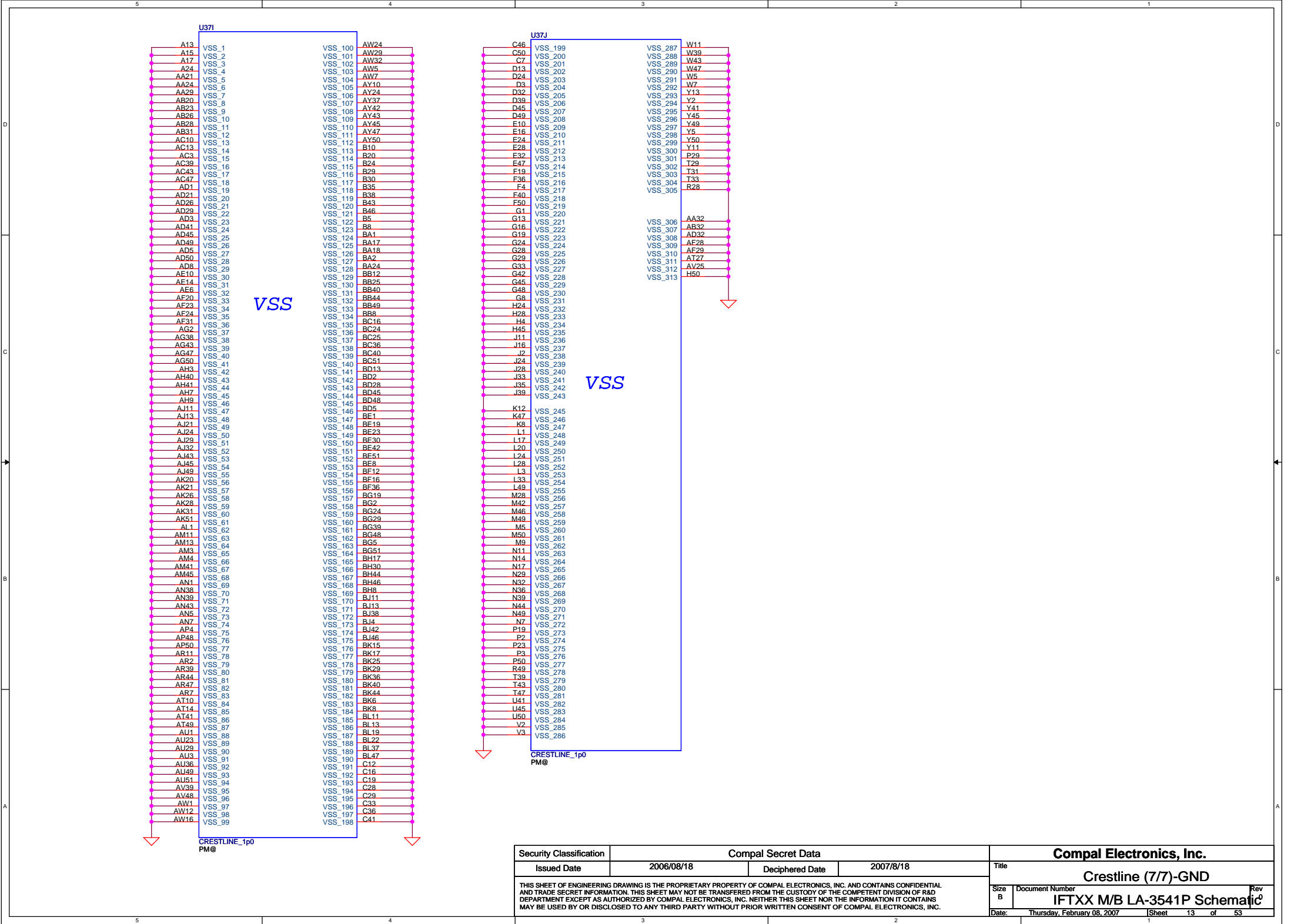


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				IFTXX M/B LA-3541P Schematic	
				Date:	Friday, February 09, 2007
				Sheet	10 of 53



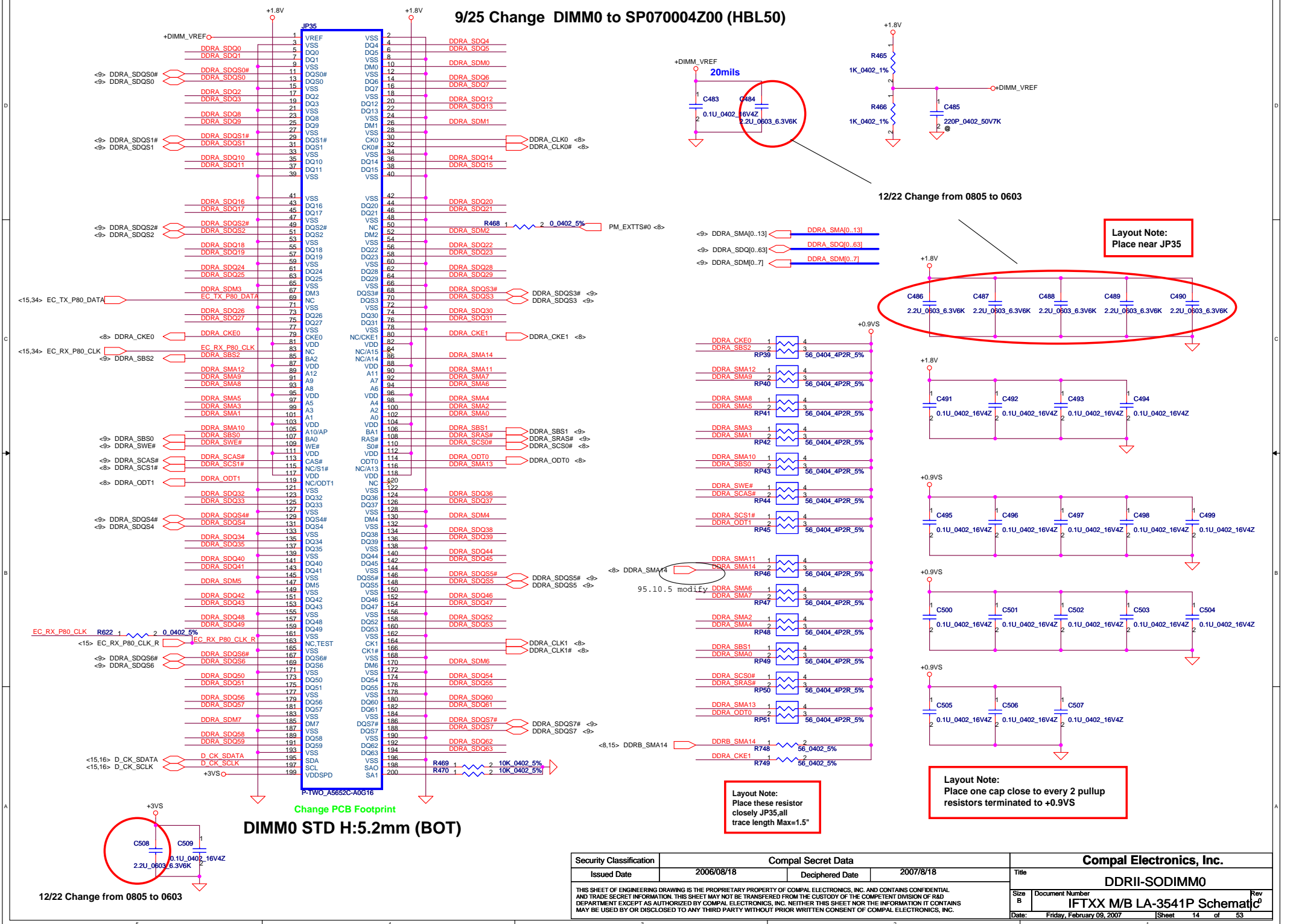




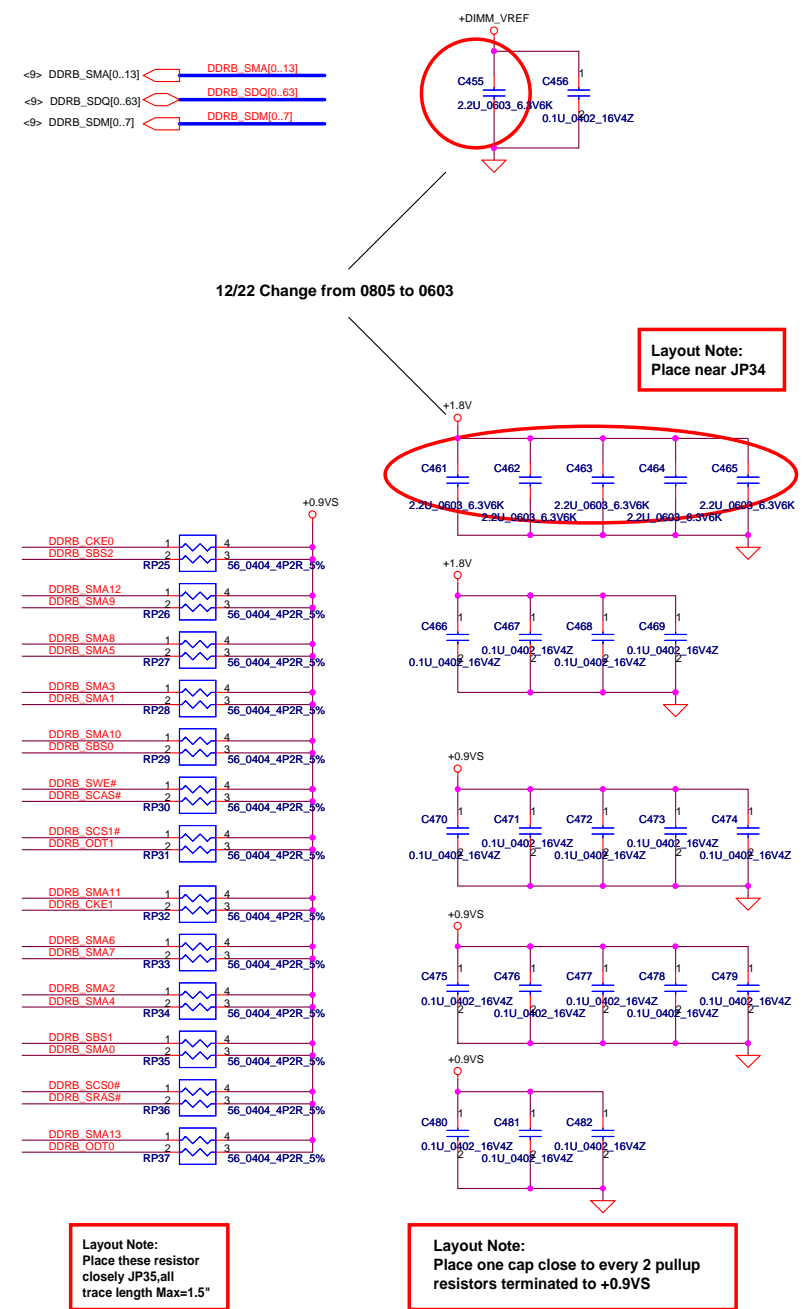


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						Size B		Document Number		Rev	
						IFTXX M/B LA-3541P Schematic					
						Date:		Thursday, February 08, 2007		Sheet 13 of 53	

# 9/25 Change DIMM0 to SP070004Z00 (HBL50)



**DIMM1 STD H:9.2mm (BOT)**



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				IF7XX M/B LA-3541P Schematic	
				Date	Friday, February 09, 2007
				Sheet	15 of 53

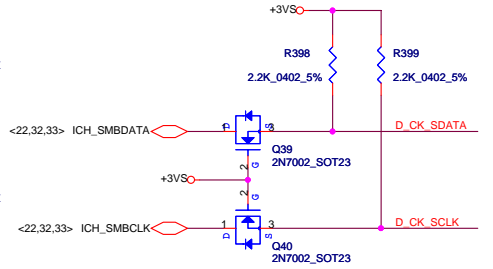
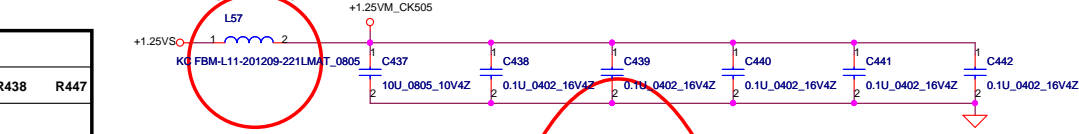


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

### FSB Frequency Selet:

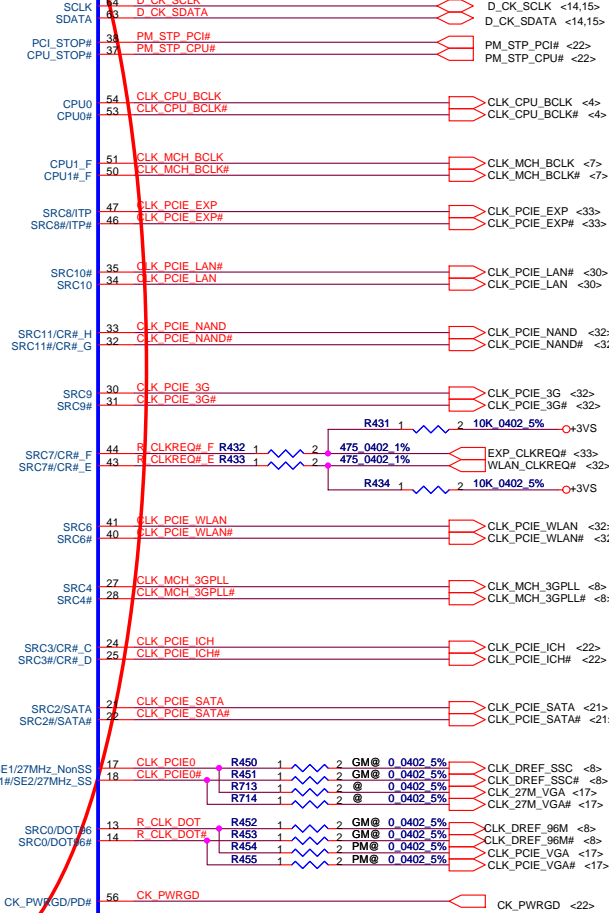
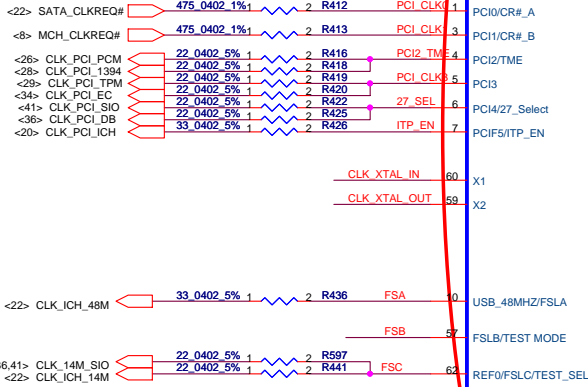
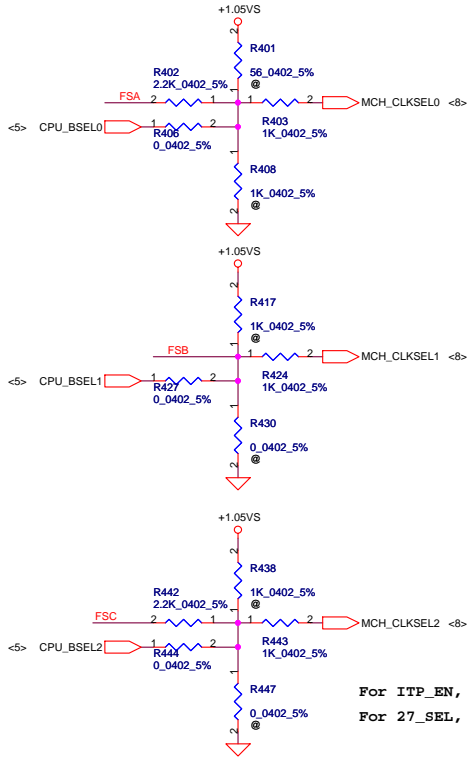
CPU Driven	Stuff						
★ (Default)	No Stuff	R401	R408	R417	R430	R438	R447
	Stuff	R401	R417	R447			
667MHz	No Stuff	R408	R430	R438			
	Stuff	R408	R417	R447			
800MHz	No Stuff	R401	R430	R438			
	Stuff	R401	R430	R438			

12/4 Modified from 0 Ohm to bead (3A rated)



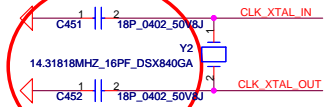
10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol



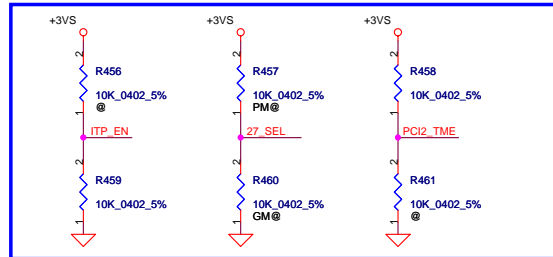
C444	2	1	CLK_ICH_48M
C445	2	1	5P_0402_50V8C
C446	2	1	4.7P_0402_50V8C
C447	2	1	CLK_PCI_ICH
C448	2	1	CLK_14M_SIO
C449	2	1	4.7P_0402_50V8C
C450	2	1	CLK_PCI_PCM
C451	2	1	CLK_PCI_EC
C452	2	1	CLK_PCI_SIO
C453	2	1	4.7P_0402_50V8C
C454	2	1	CLK_PCI_SIO
C455	2	1	4.7P_0402_50V8C

Place close to U35







12/1 Modified from 27P to 18P

Routing the trace at least 10mil



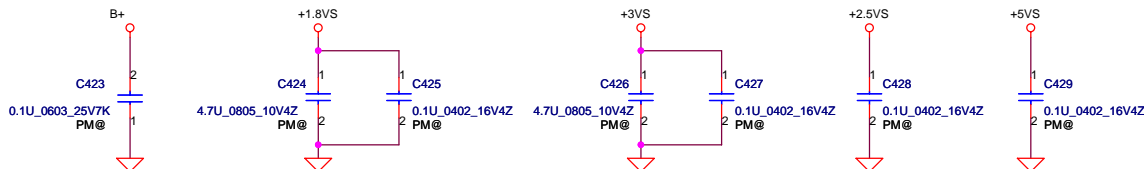
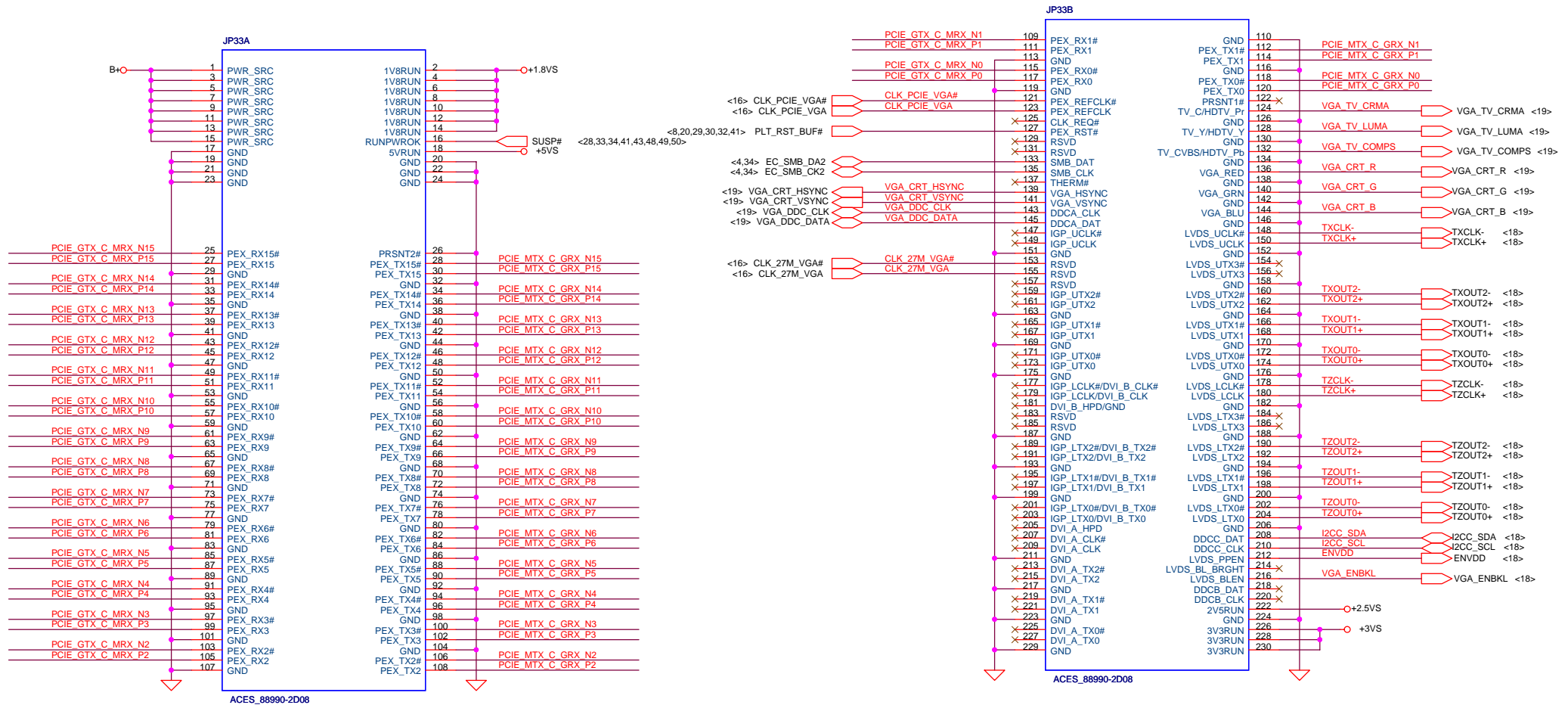
Security Classification	Compal Secret Data	Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Date: Friday, February 09, 2007		Sheet	16 of 53

<10> PCIE\_MTX\_C\_GRX\_N[0..15]  PCIE\_MTX\_C\_GRX\_N[0..15]  
<10> PCIE\_MTX\_C\_GRX\_P[0..15]  PCIE\_MTX\_C\_GRX\_P[0..15]  
<10> PCIE\_GTX\_C\_MRX\_N[0..15]  PCIE\_GTX\_C\_MRX\_N[0..15]  
<10> PCIE\_GTX\_C\_MRX\_P[0..15]  PCIE\_GTX\_C\_MRX\_P[0..15]

9/13 modify this footprint from ACES\_88990-2D08\_230P to ACES\_88990-2D28\_230P

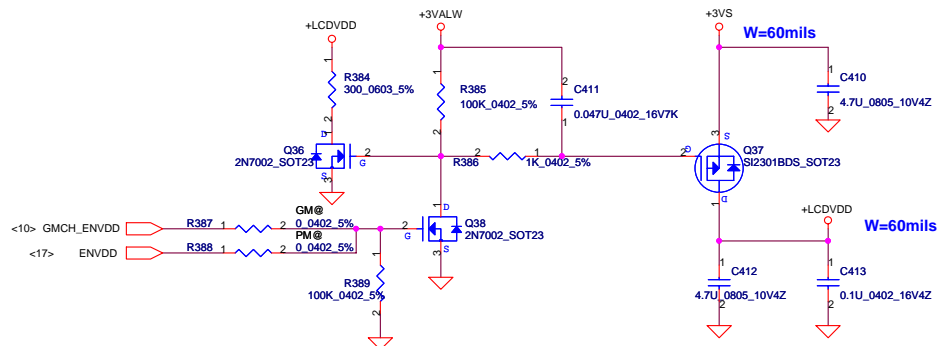
12/19 modify this footprint from ACES\_88990-2D28\_230P to QUASA\_CA0330-230N20\_230P

0208 : Modify this footprint from QUASA\_CA0330-230N20\_230P to QUASA\_CA0330-230N20\_230P-S

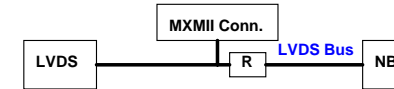


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		Date	
Custom	IFTXX M/B LA-3541P Schematic			Friday, February 09, 2007	
Sheet		17		of	
53					

# LCD POWER CIRCUIT

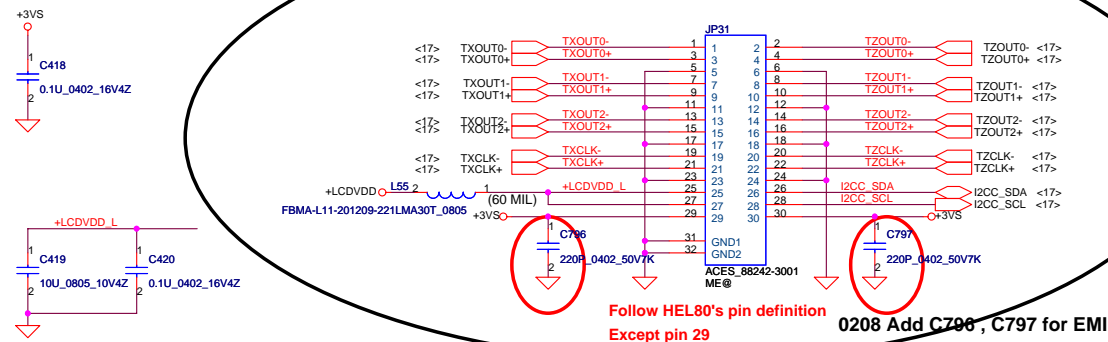


## Routing Diagram

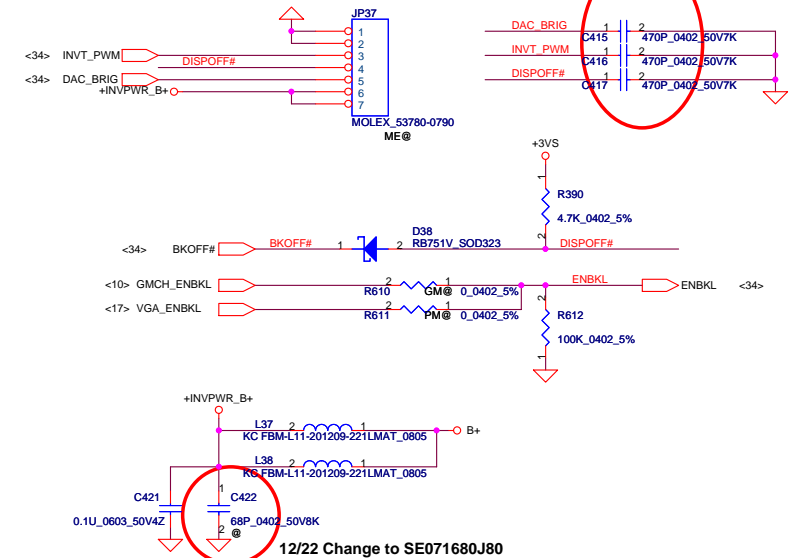


Use Daisy chain to route

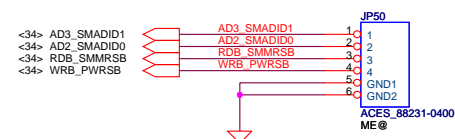
## LCD/PANEL BD. Conn.



## INVERTER Conn.

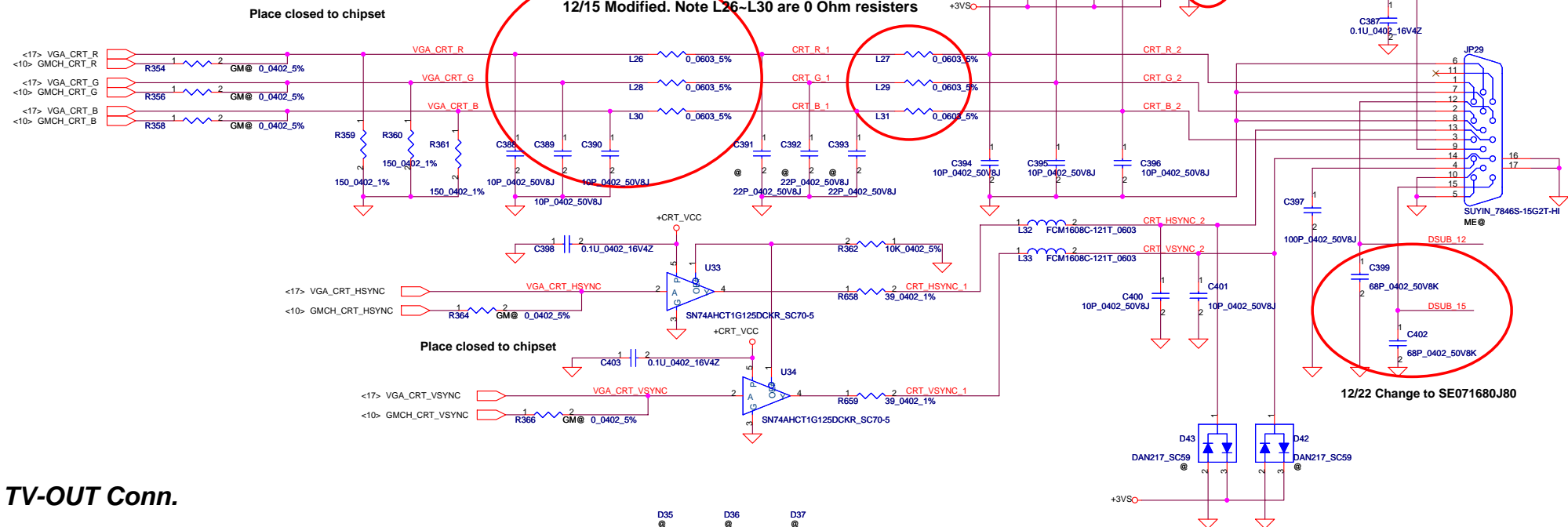


## JEPICO Conn.

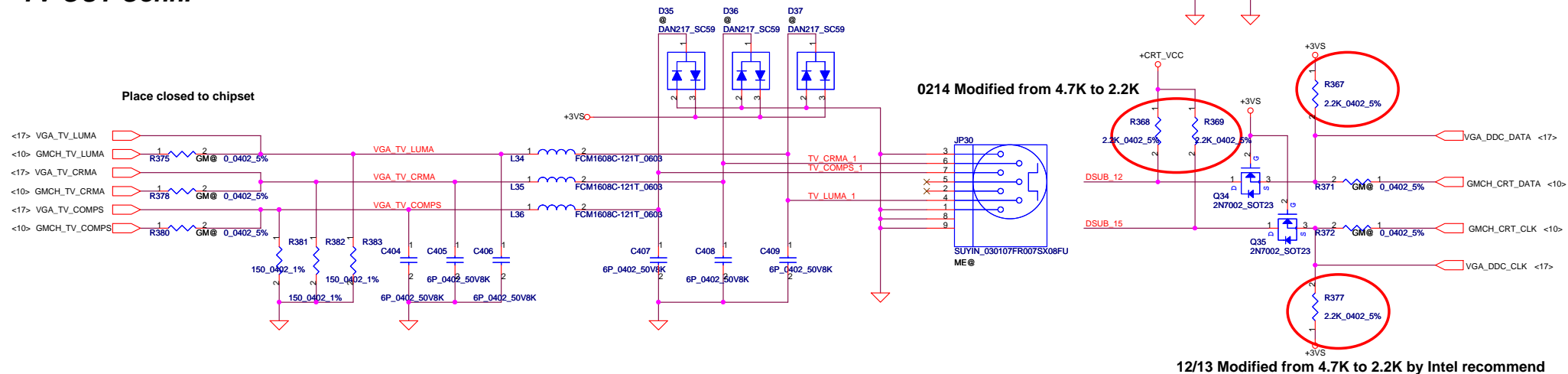


Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	LVDS & DVI Connector	
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				IFTXX M/B LA-3541P Schematic	
				Date: Friday, February 09, 2007	Sheet 18 of 53

# CRT Connector



## TV-OUT Conn.



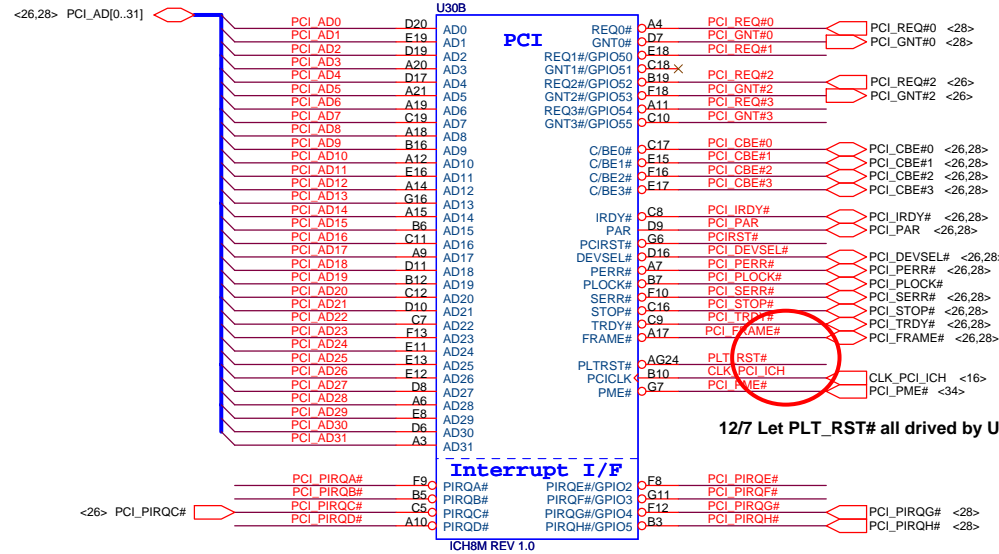
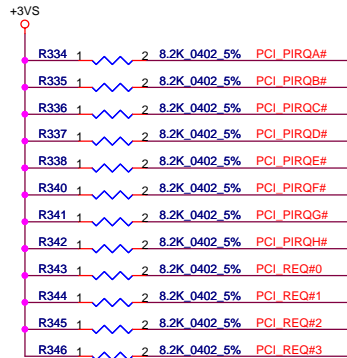
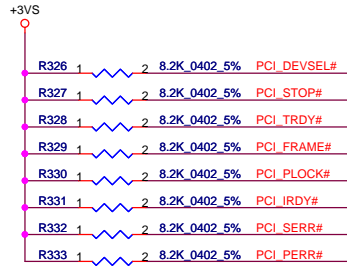
Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	CRT & TV-OUT Connector	
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				IFTXX M/B LA-3541P Schematic	
				Date: Thursday, February 15, 2007	Sheet 19 of 53

10/17 : Change P/N from SA000010G00 to SA00001JU10

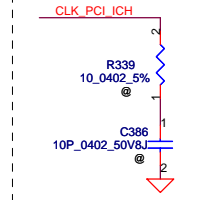
10/17 : FootPrint : SA000010G00

BOM : SA00001JU10

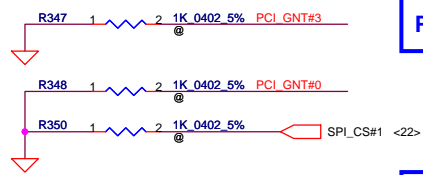
1/2 : Change U37 GM part number to SA00001JU80



Place closely pin B10

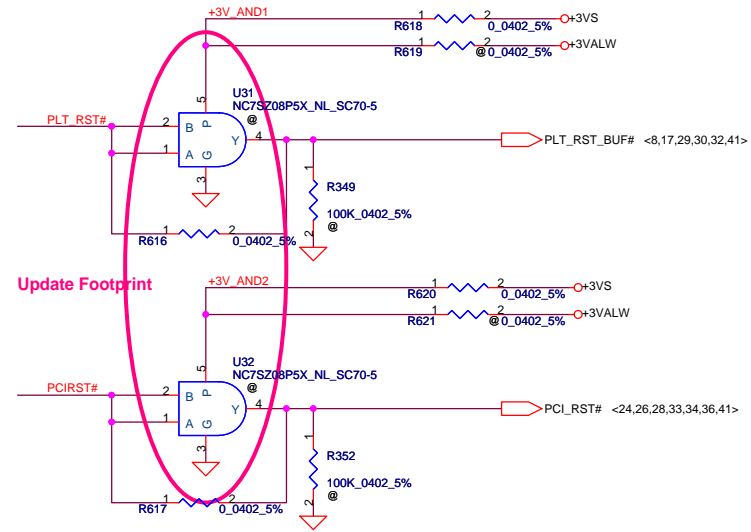


12/7 Let PLT\_RST# all driven by U31



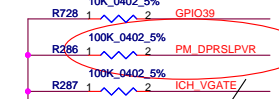
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

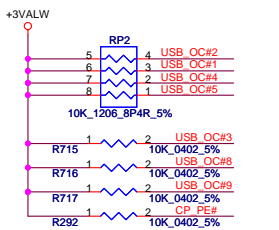




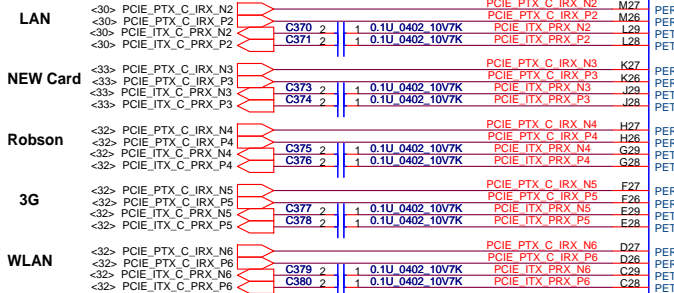
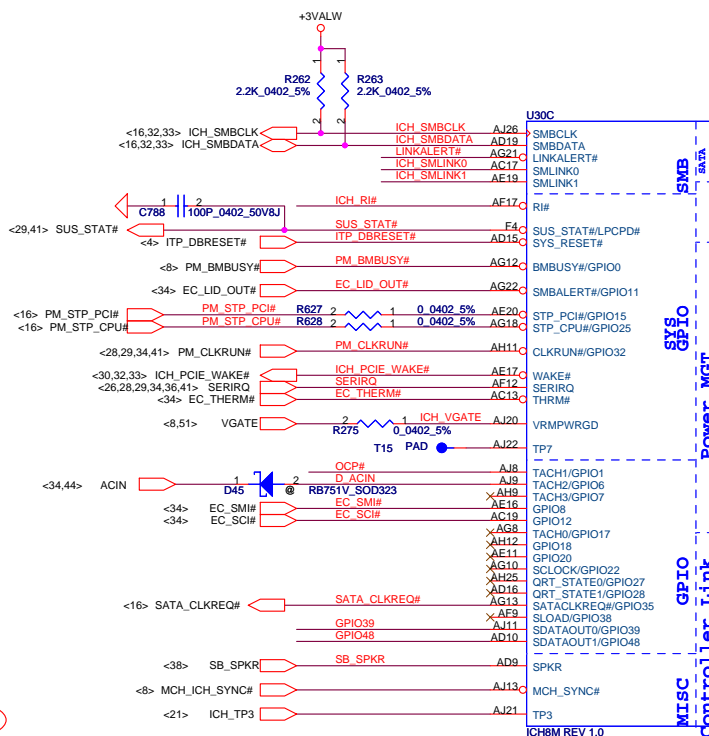
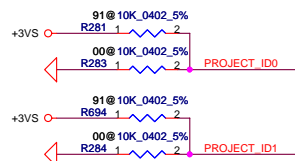




Not in CRB,Keep!

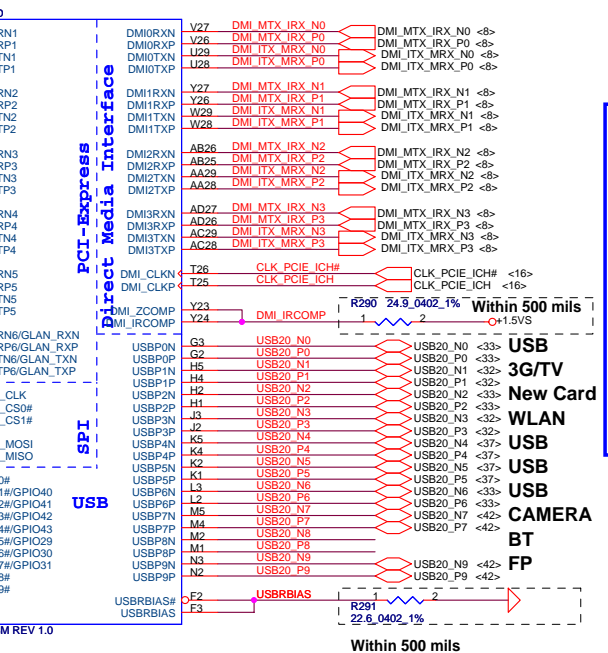
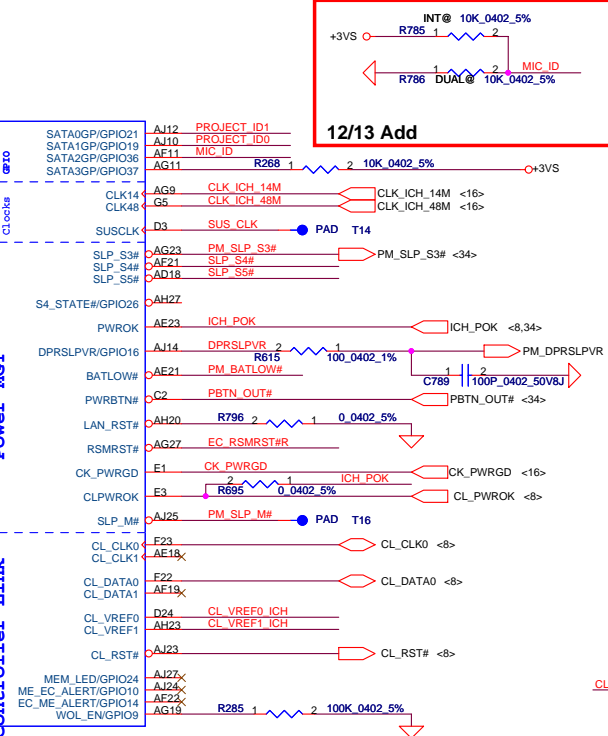
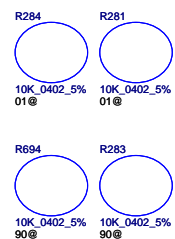


	ID1	ID0
IFT00 ( 00 )	R284	R283
IFT01 ( 01 )	R284	R281
IFL90 ( 10 )	R694	R283
IFT91 ( 11 )	R694	R281

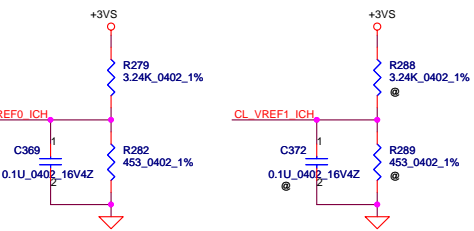
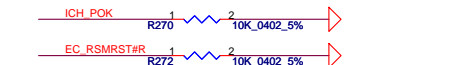
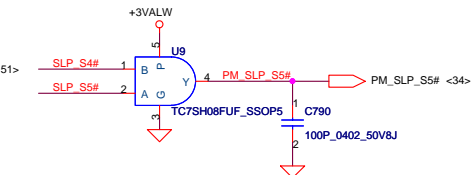
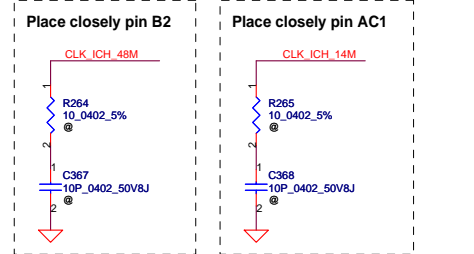


SPI not used, Left NC

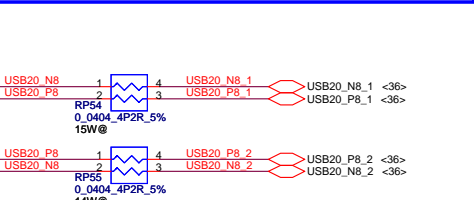
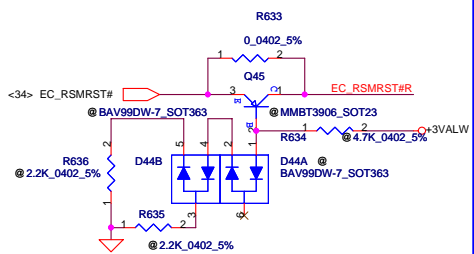
**12/1 Modified**



**Within 500 miles**

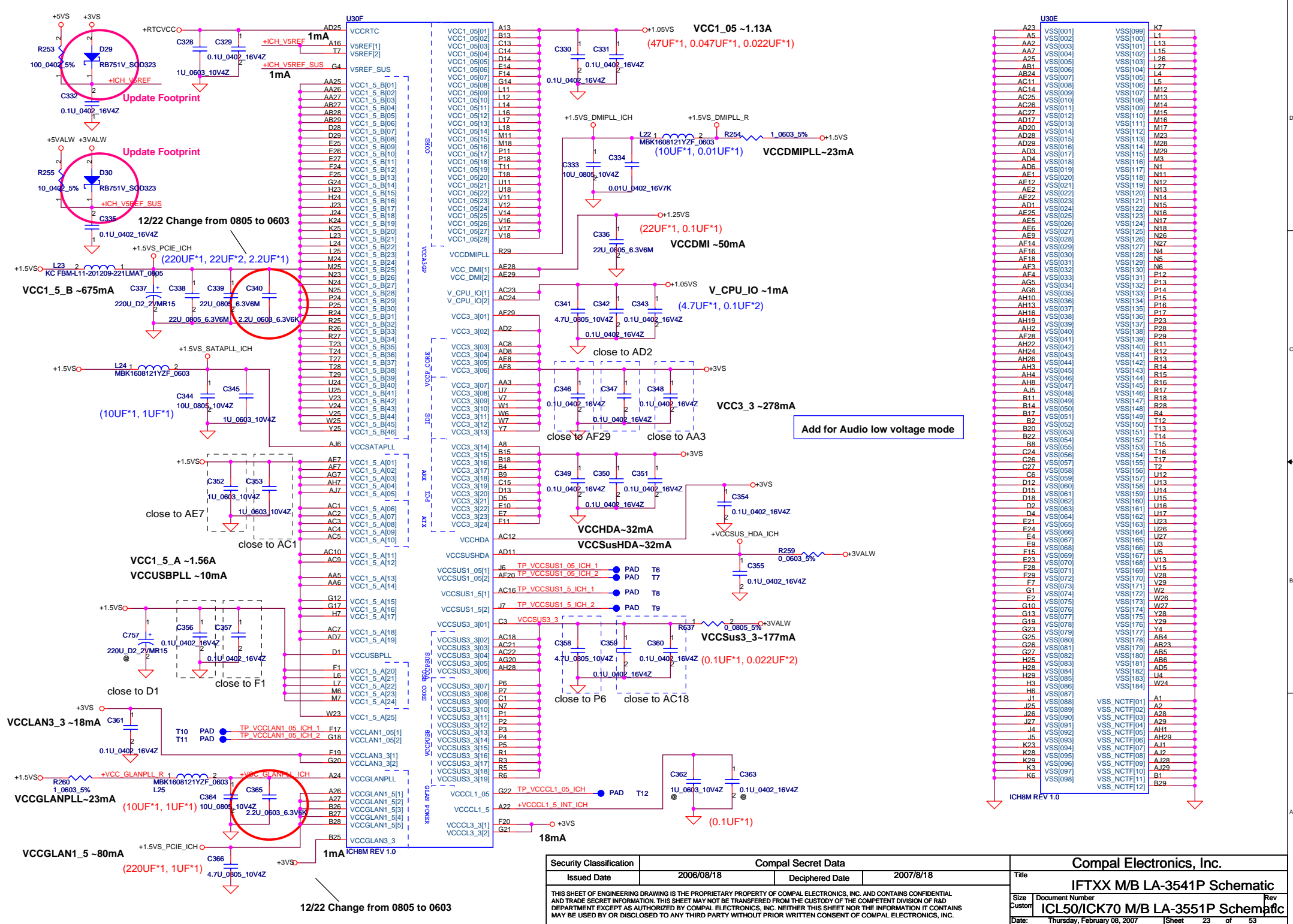


## RSMRST circuit



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						Size	Document Number				Rev
						Custom	IFTXX M/B LA-3541P Schematic				0
						Date:	Wednesday, February 14, 2007		Sheet	22	of 53



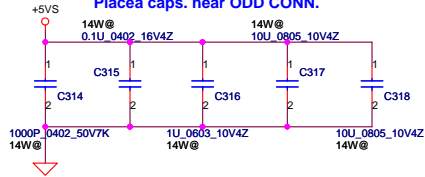


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Issued Date	2006/08/18	Deciphered Date	2007/8/18
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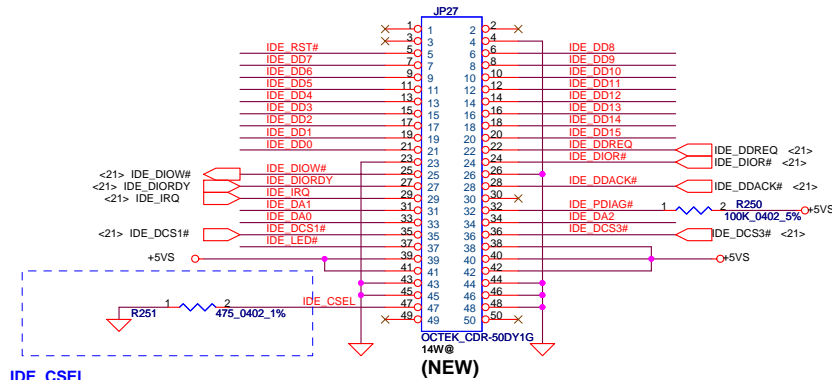
Compal Electronics, Inc.		
Title		
I/FTXX M/B LA-3541P Schematic		
Size	Document Number	Rev
Custom	ICL50/ICK70 M/B LA-3551P Schematic	
Date	Thursday, February 08, 2007	Sheet 23 of 53

## 14W ODD Conn.

Place caps. near ODD CONN.



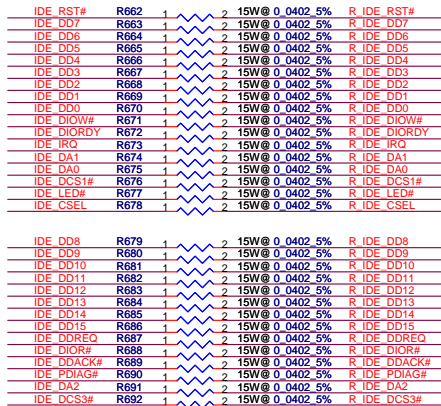
<21> IDE\_DD[0..15] IDE\_DD[0..15]  
<21> IDE\_DA[0..2] IDE\_DA[0..2]



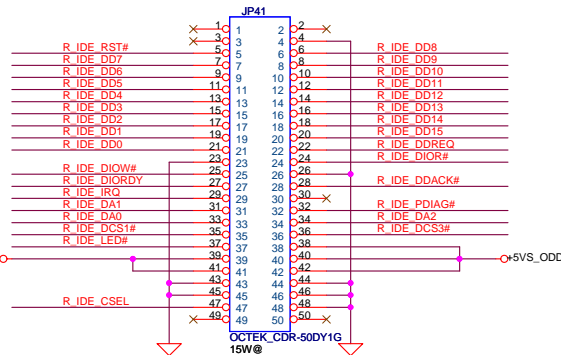
IDE\_CSEL  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)

+5VS R252 100K\_0402\_5%

## 15W ODD Conn.

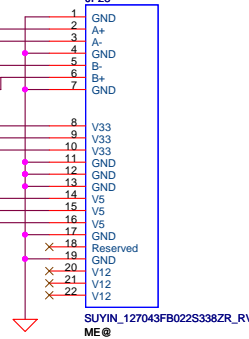
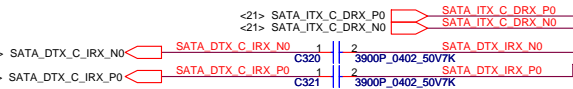
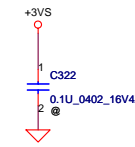
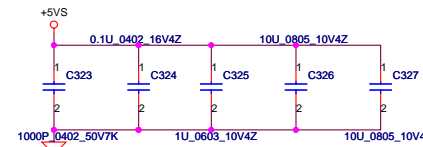


+5VS\_ODD



12/4 Change J7 to 2x0 Ohm 1/4w resistors

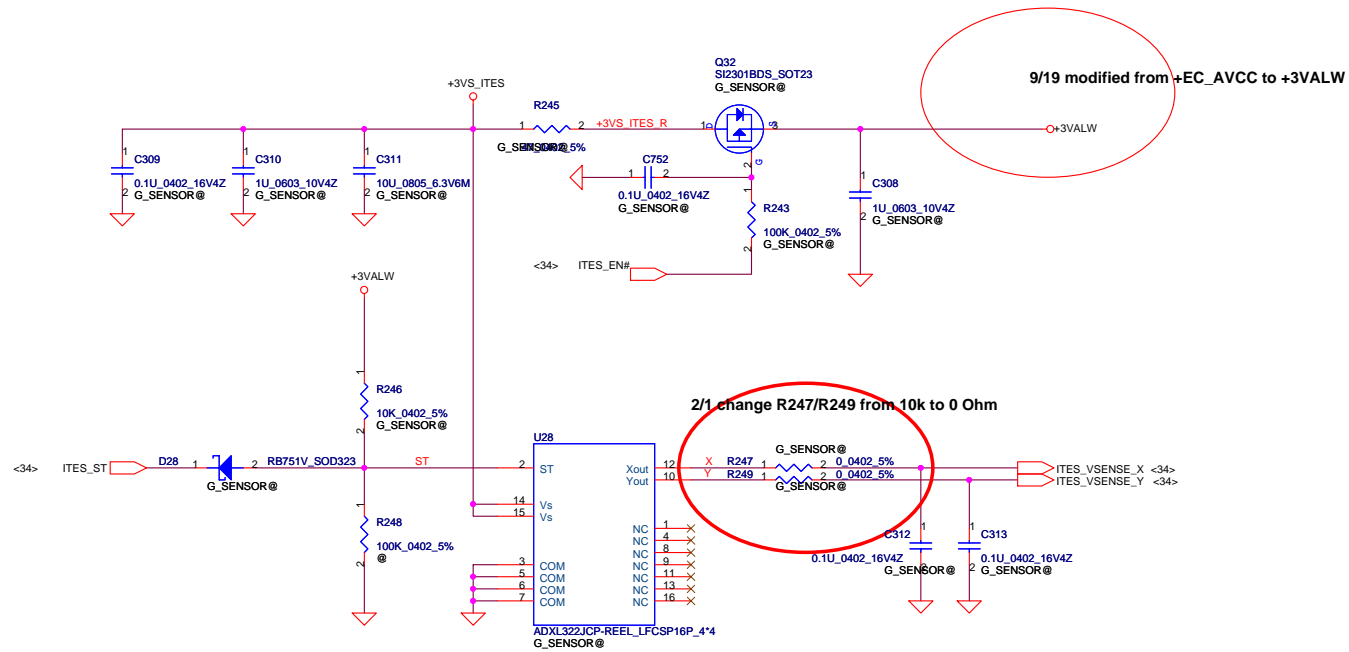
## SATA HDD Conn.



(NEW)  
Change Library

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Deciphered Date				2007/8/18				HDD & ODD Connector			
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								IFTXX M/B LA-3541P Schematic			
								Date: Thursday, February 08, 2007			
								Sheet 24 of 53			

0206 => Note : Change BOM structure from HS@ to G-SENSOR@



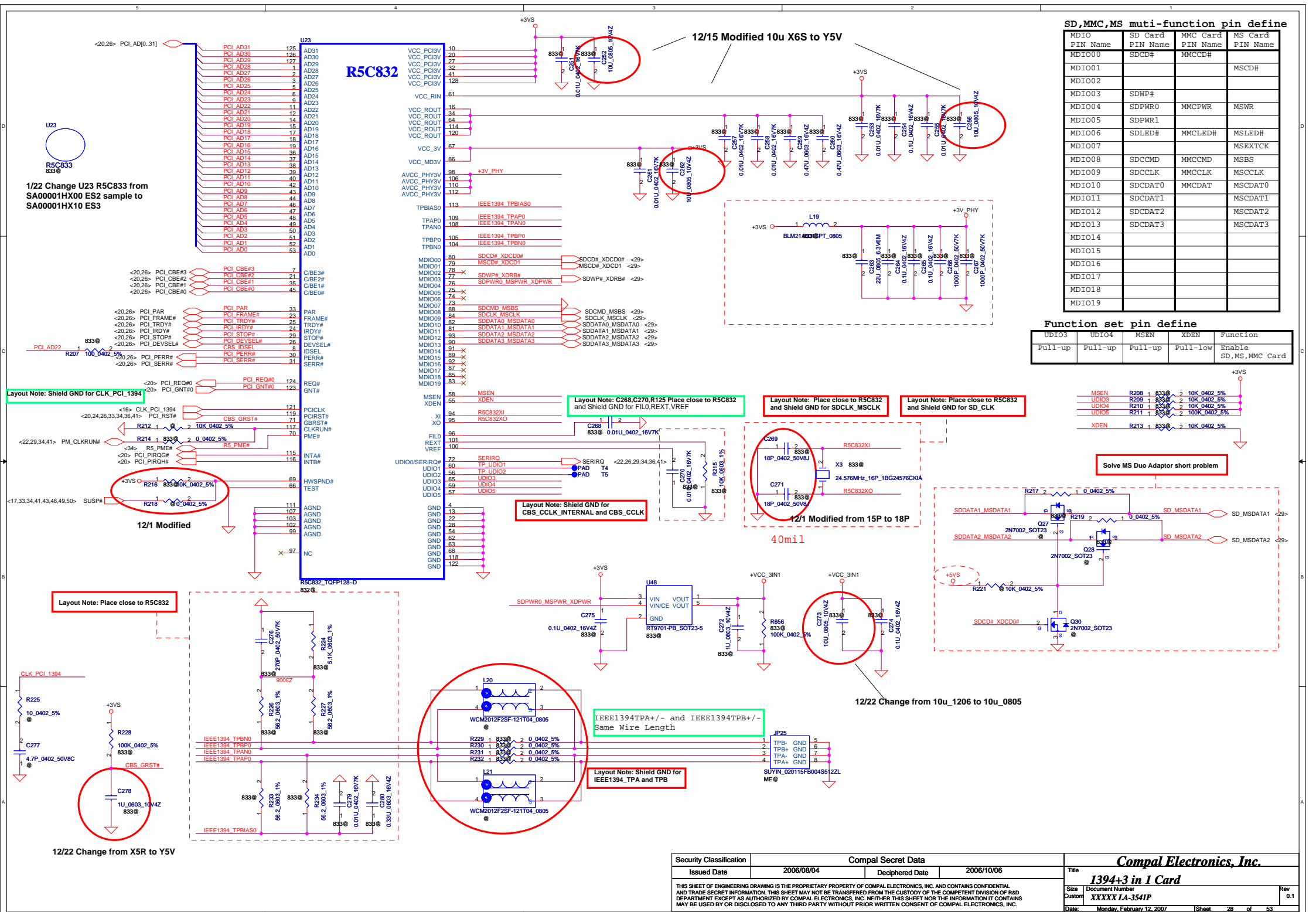
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	
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Size B	Document Number	LA-3541P			Rev 0.1
Date: Tuesday, February 13, 2007		Sheet 25 of 53			



5					4					3					2					1				
D																								
C																								
B																								
A																								

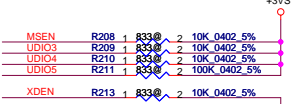
Title																													
<Title>																													
Size		Document Number																				Rev							
A		<Doc>																				<RevCoo							
Date:										Thursday, February 08, 2007										Sheet					27 of 53				

Title									
<Title>									
Size	Document Number								Rev
A	<Doc>								<Rev
Date:	Thursday, February 08, 2007					Sheet	27	of	53

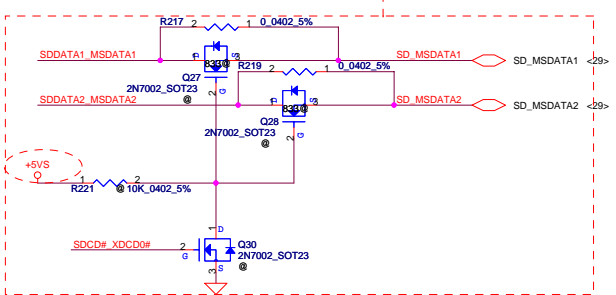


SD,MMC,MS multi-function pin define			
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
MDIO00	SDCD#	MMCCD#	
MDIO01			MSCD#
MDIO02			
MDIO03	SDWP#		
MDIO04	SDPWR0	MMCPWR	MSWR
MDIO05	SDPWR1		
MDIO06	SLEED#	MMCLEED#	MSLEED#
MDIO07			MSEXTCK
MDIO08	SDCCMD	MMCCMD	MSBS
MDIO09	SDCLK	MMCLK	MSCCLK
MDIO10	SDCDAT0	MMCDAT	MSCDAT0
MDIO11	SDCDAT1		MSCDAT1
MDIO12	SDCDAT2		MSCDAT2
MDIO13	SDCDAT3		MSCDAT3
MDIO14			
MDIO15			
MDIO16			
MDIO17			
MDIO18			
MDIO19			

Function set pin define			
UDIO3	UDIO4	MSEN	XDEN
Pull-up	Pull-up	Pull-up	Pull-low
			Enable
			SD,MS,MMC Card

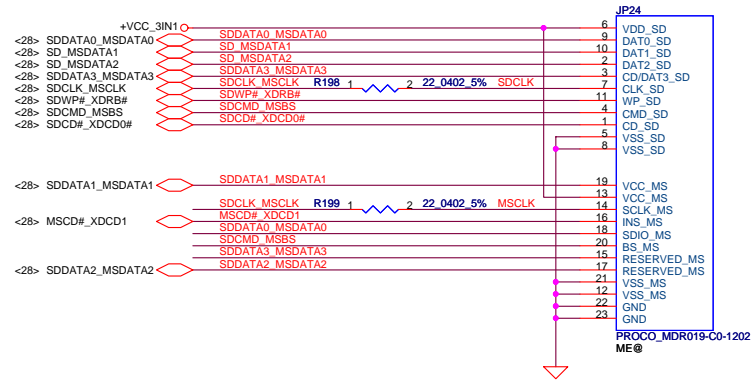


Solve MS Duo Adaptor short problem

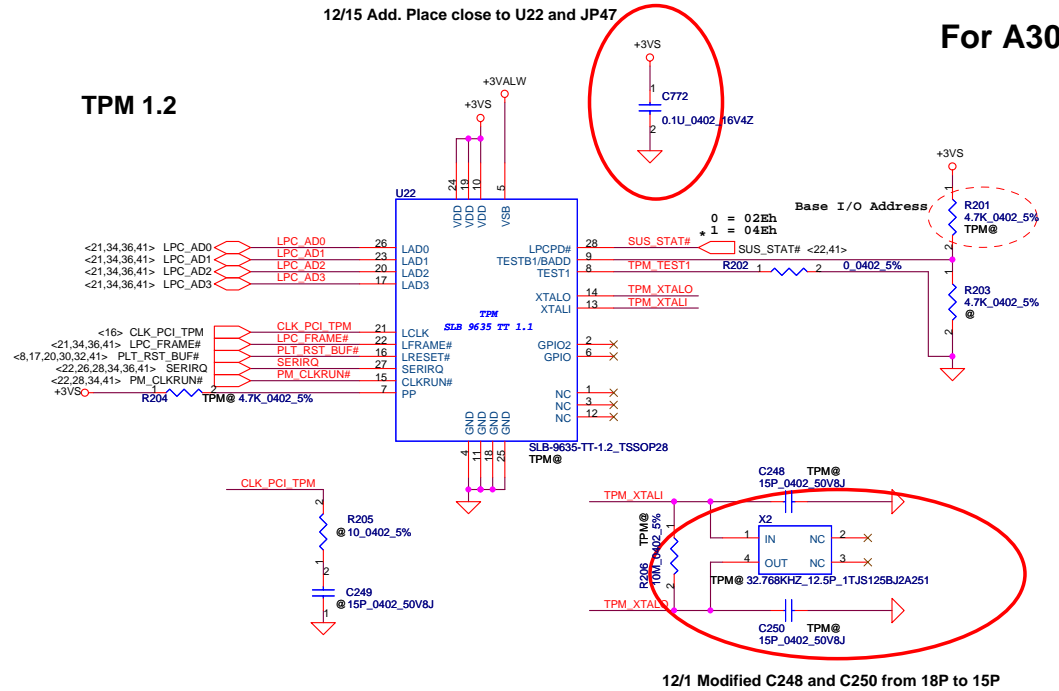


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Title		Compal Electronics, Inc.	
Size		1394-3 in 1 Card	
Customer		XXXXX LA-3541P	
Date		Monday, February 12, 2007	
Sheet		28 of 53	
Rev		0.1	

### 3 in 1 Card Reader

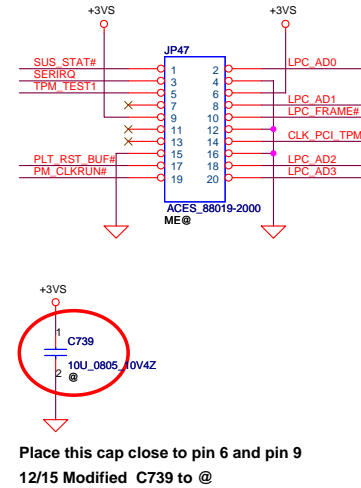


### TPM 1.2



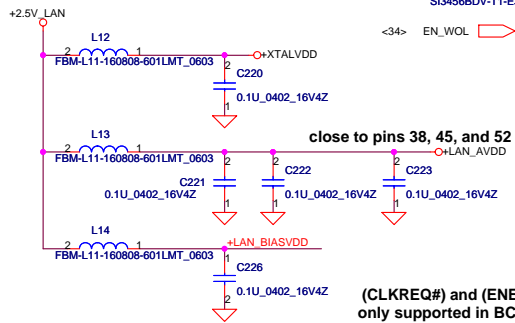
For A30

TPM Conn. For C38

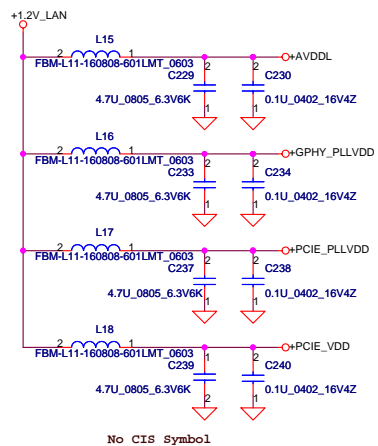




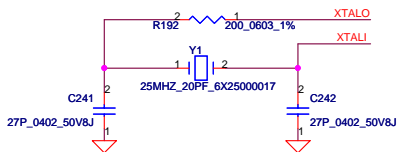
Layout Notice : Filter place as close chip as possible.



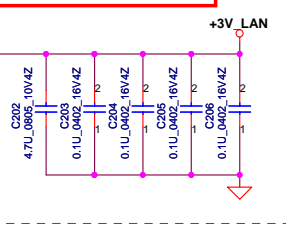
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



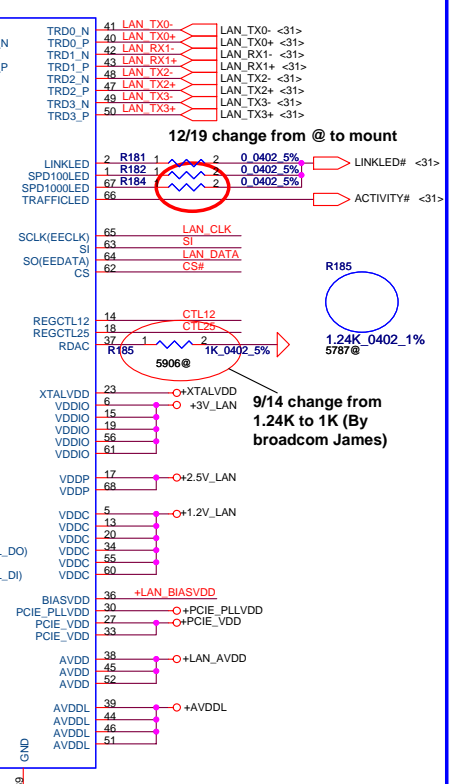
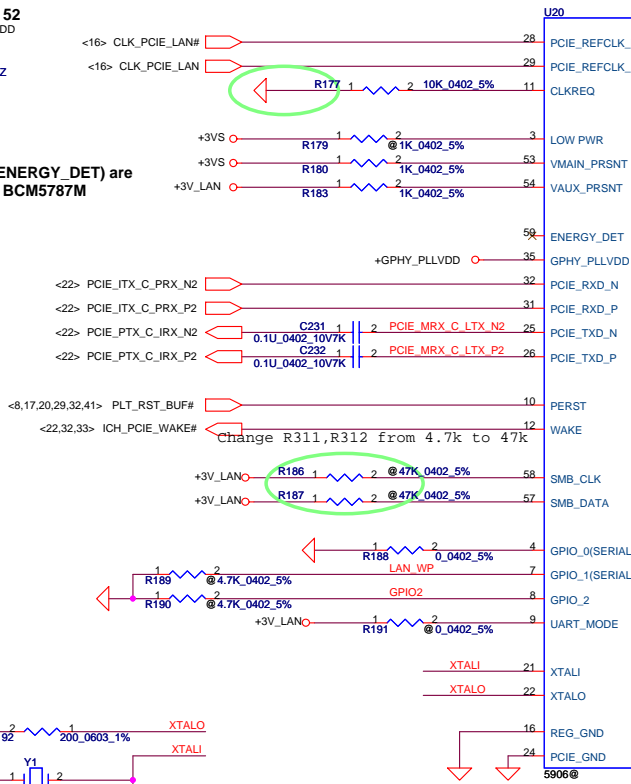
No CIS Symbol



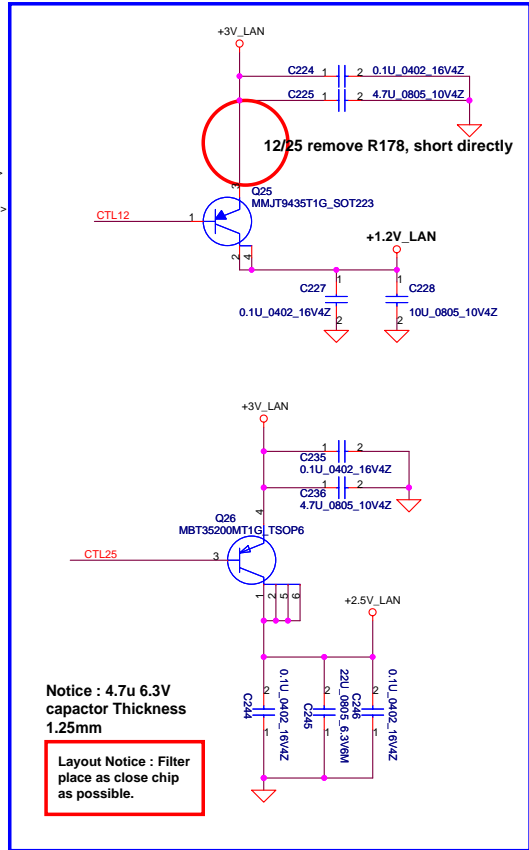
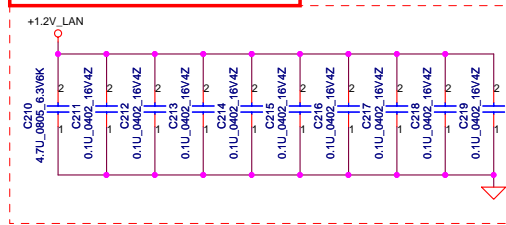
Layout Notice : Place as close chip as possible.



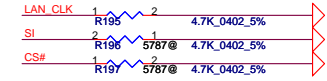
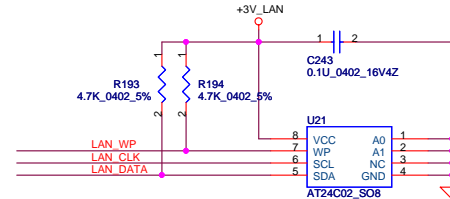
12/26 change 5906 pn to SA00001I010 (A2)  
5787 is already A2 version



Layout Notice : 1.2V filter. Place as close chip as possible.

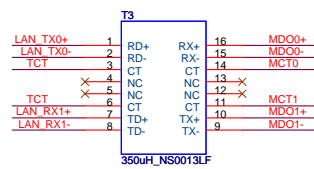
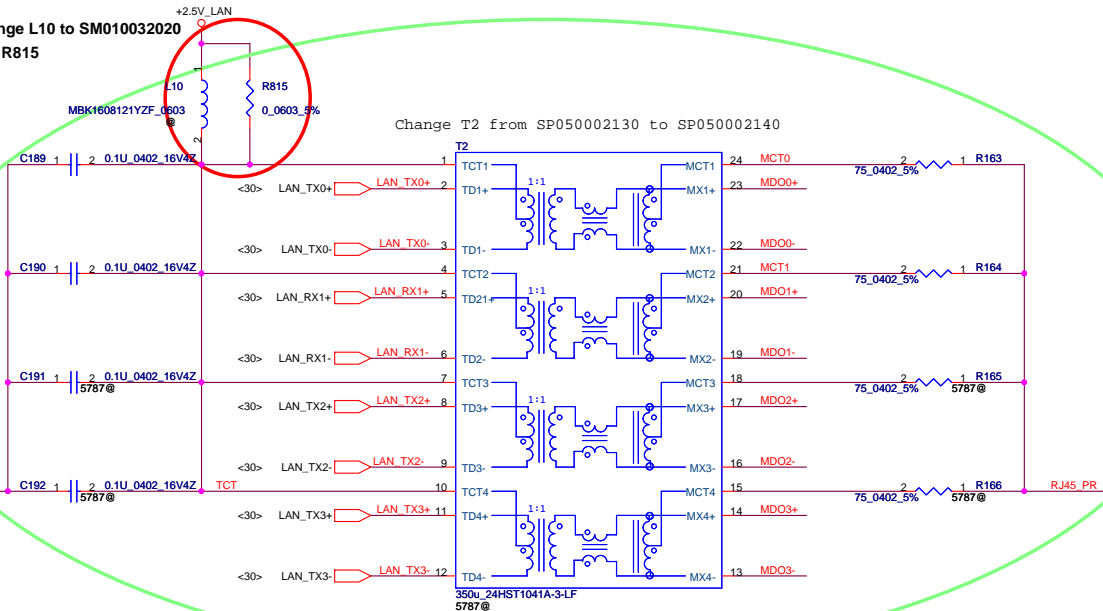


Layout Notice : Filter place as close chip as possible.



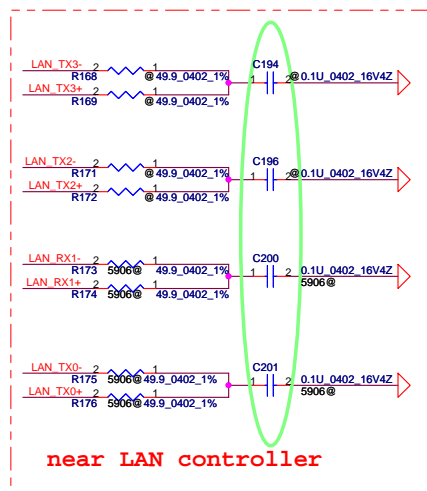
Security Classification				Compal Secret Data				Title			
Issued Date				2006/08/04				Deciphered Date			
2006/10/06				2006/10/06				BCM5787MKML			
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Date: Thursday, February 15, 2007				Sheet 30 of 53				Rev 0.1			

12/27 Change L10 to SM010032020  
12/27 Add R815

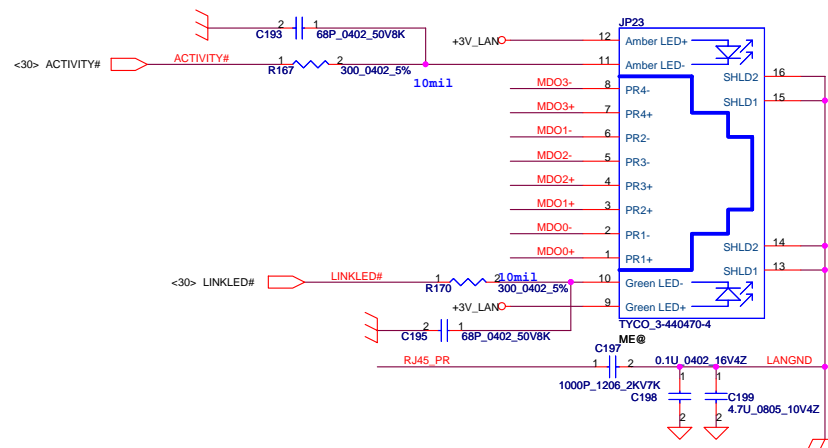


Change T1 from SP050001210 to SP050001210

Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF

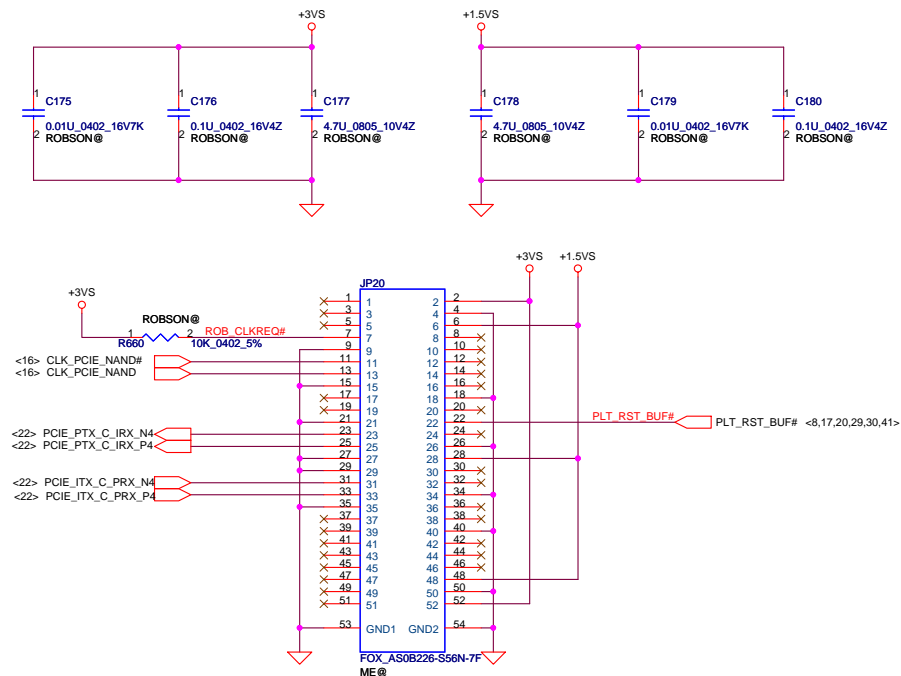


**Lan Conn.**

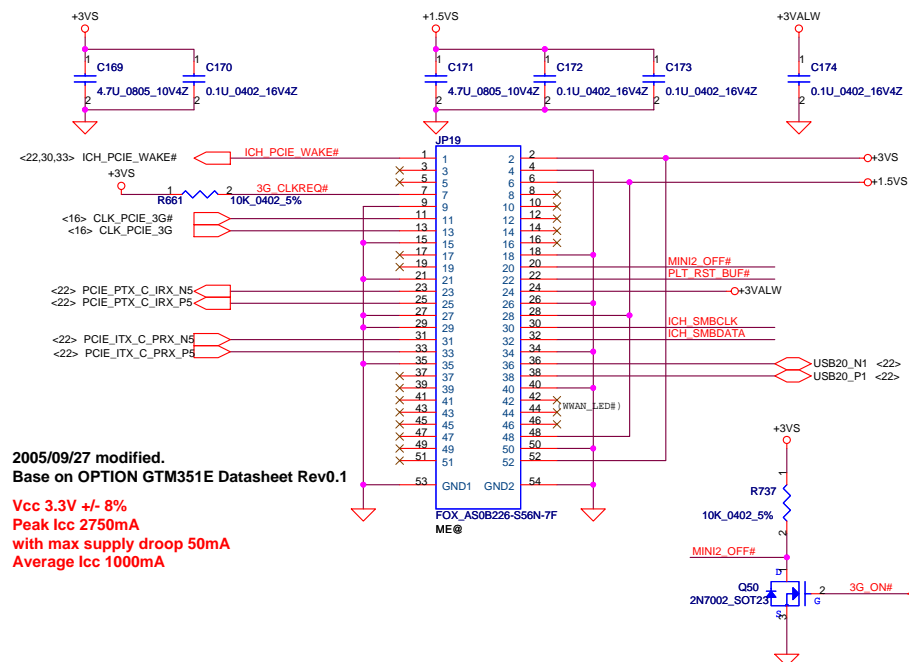


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						Size	Document Number				Rev
						Custom	XXXXX LA-354P				0.
						Date:	Thursday, February 08, 2007		Sheet	31	of 53

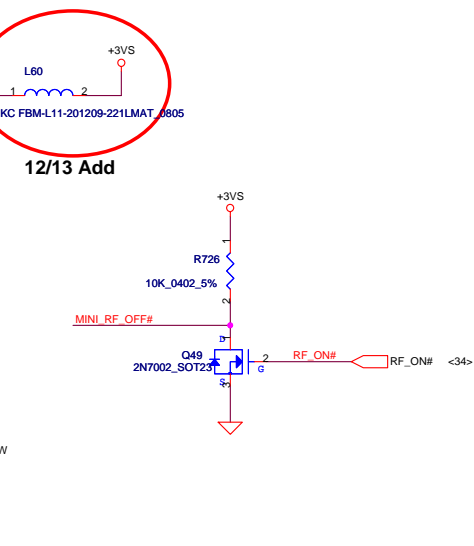
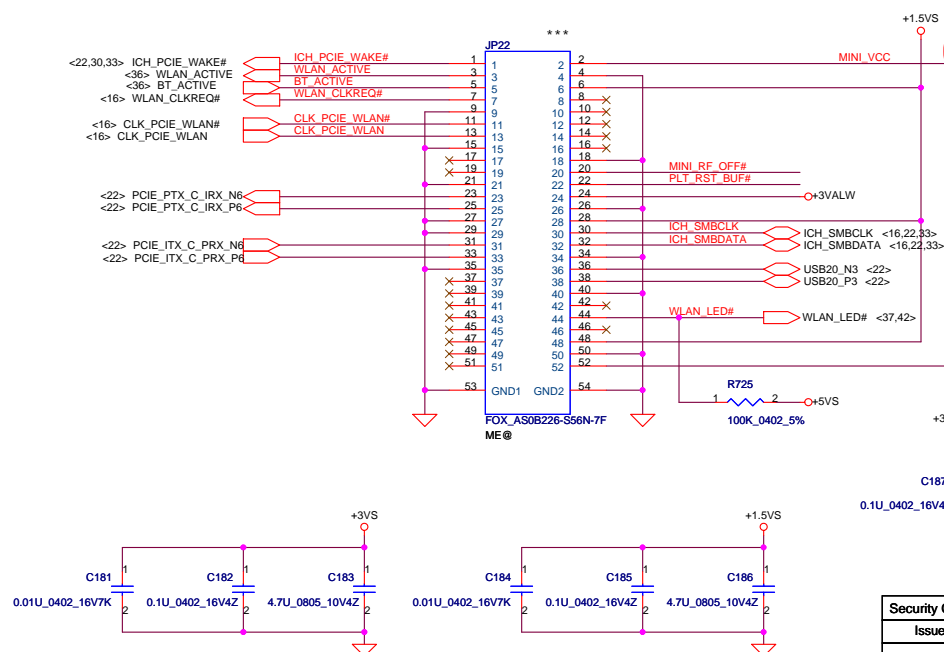
## NAND mini Card(Robson support)



## Mini-Express Card for 3G Or TV Tuner

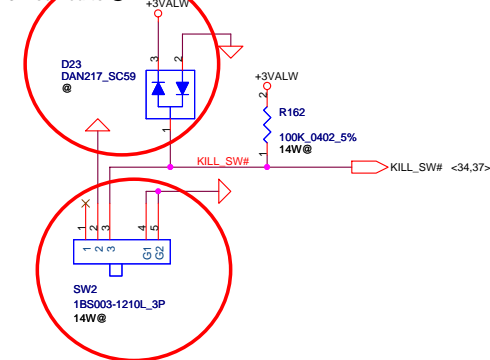


## Mini-Express Card for WLAN



## Kill SWITCH

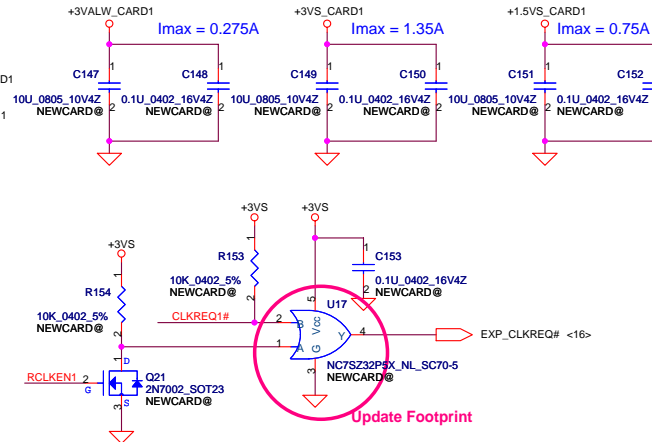
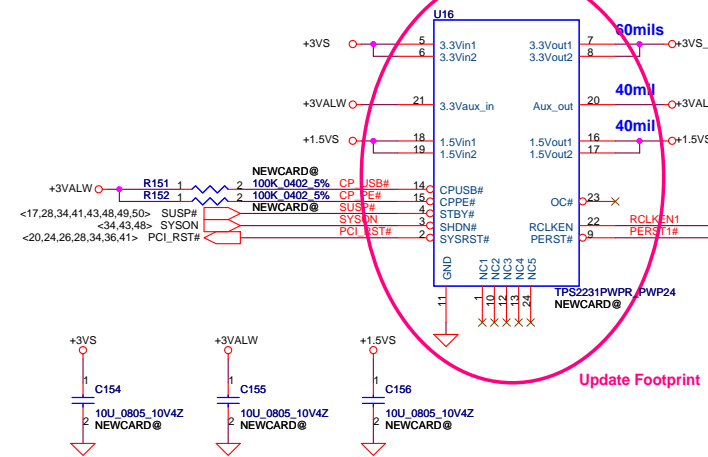
12/28 modified to @



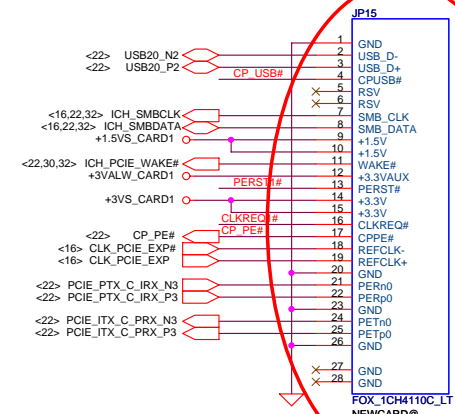
12/19 Change SW2 to correct symbol (by EMI)

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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title		
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				Size	Document Number	Rev
				LA-3541P		
Date:				Friday, February 09, 2007	Sheet	32 of 53

## New Card Power Switch

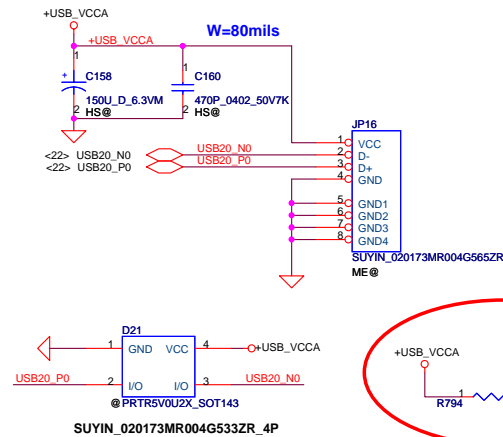


## New Card Socket (Left/TOP)

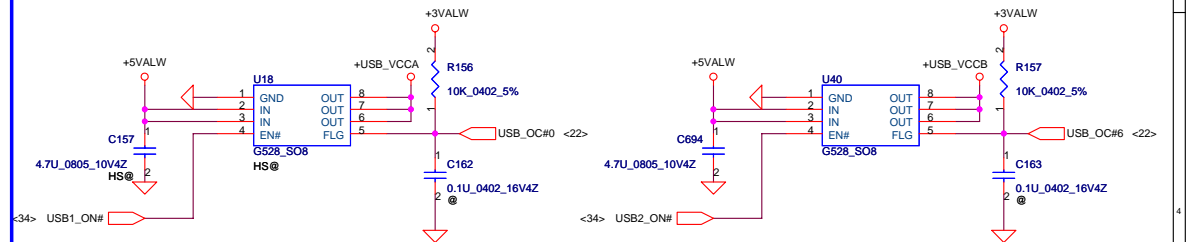
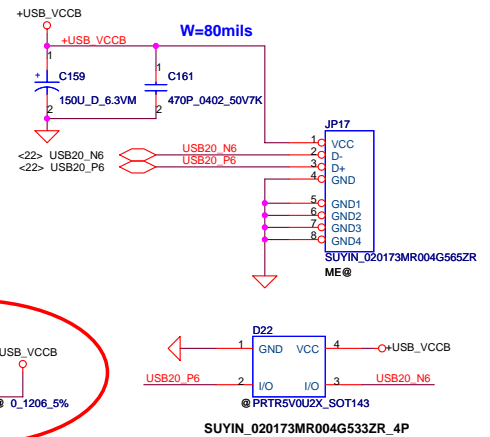


12/7 Let pin 28 dummy by EMI request  
12/13 Let pin 27 dummy by layout request  
12/27 change JP 15 footprint to FOX\_1CX41201\_26P\_LT-S

## USB CONN. 1

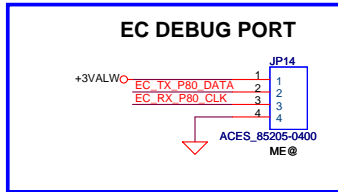
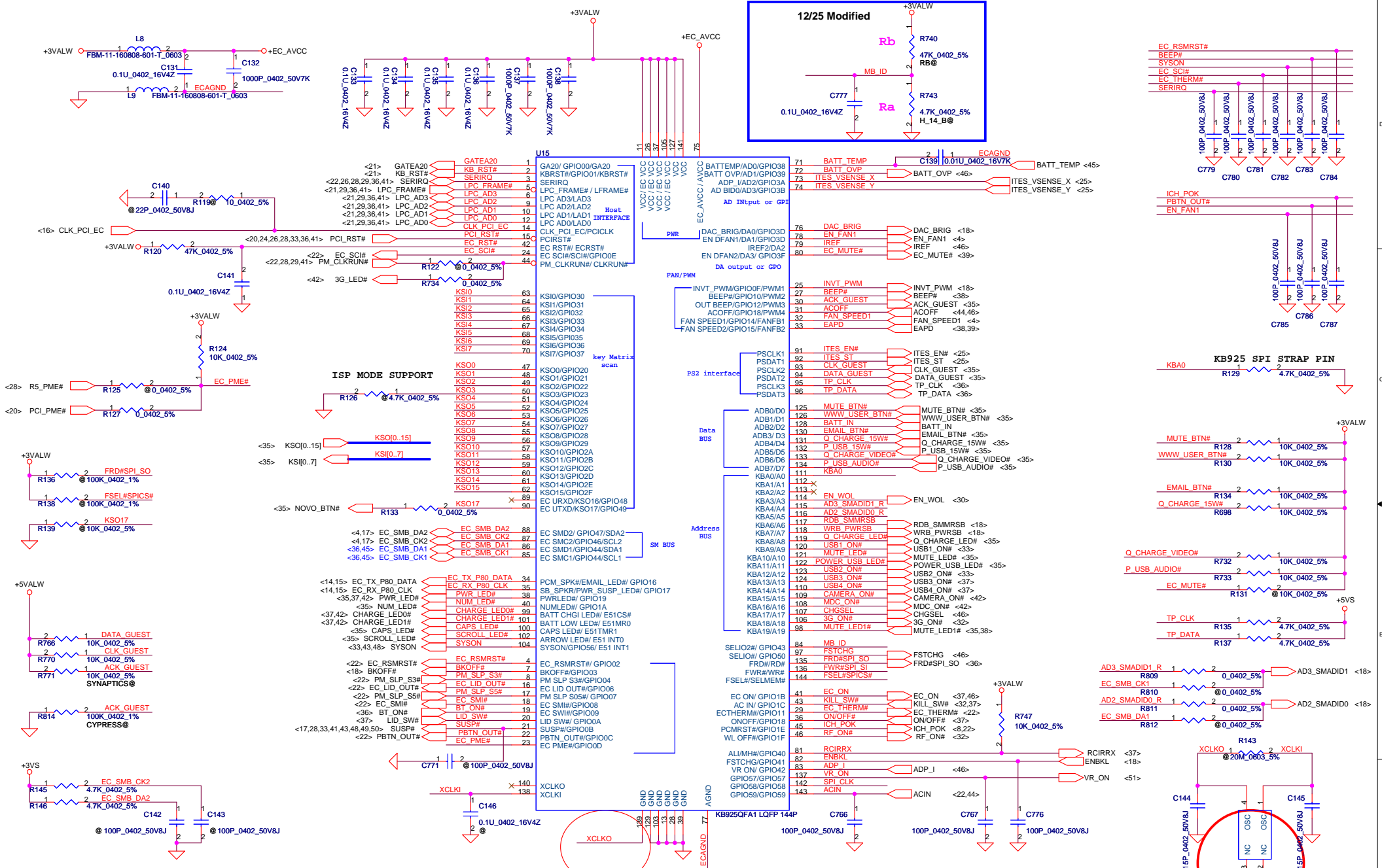


## USB CONN. 2



9/17 modified this block

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	NEW CARD & USB Connector	
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				Date: Friday, February 09, 2007	Sheet 33 of 53

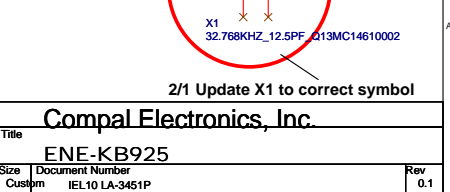


<36> SPI\_CS# 1 2 FSEL#SPICS#  
<36> SPI\_CLK\_R 1 2 SPI\_CLK  
<36> SPI\_SI 1 2 FVNR#SPI\_SI

**EC DEBUG PORT**

+3VALW 1 2 3 4  
EC\_TX\_P80\_DATA  
EC\_RX\_P80\_CLK  
ACES\_85205-0400  
ME@

0206 => Change EC part number to SA00001HZ20  
12/18 Change EC part number to SA00001HZ10  
From ver. A1 to B0

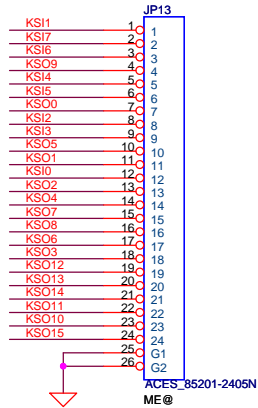


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Issued Date	2006/08/04	Deciphered Date	2006/10/06
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Title		Compal Electronics, Inc.	
ENE-KB925		Rev 0.1	
Size	Document Number	IEL10 LA-3451P	
Date:	Friday, February 09, 2007	Sheet	34 of 53

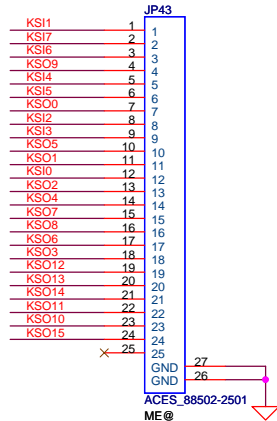
KB925 should use Data code 06361 which has fixed bonding issue  
KB925 pin 139 is used for XCLKO, Pin 140 NC

# INT\_KBD Conn.

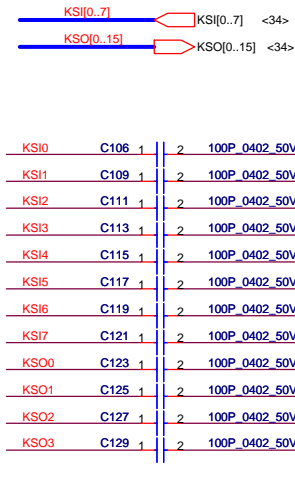
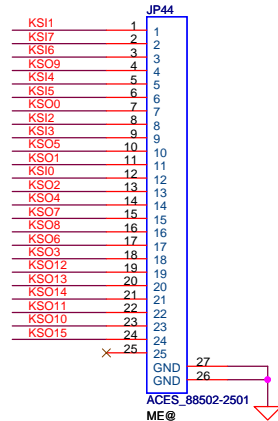
## For IFT10



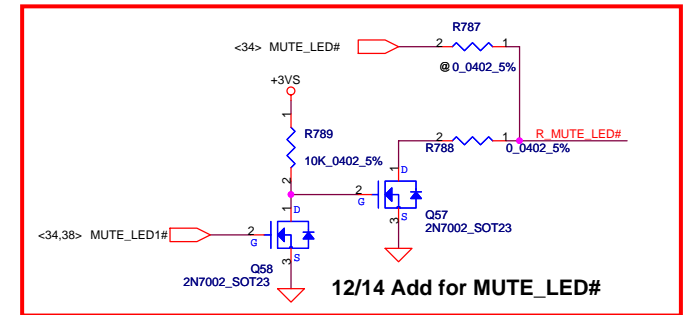
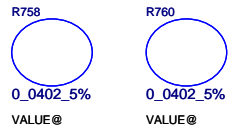
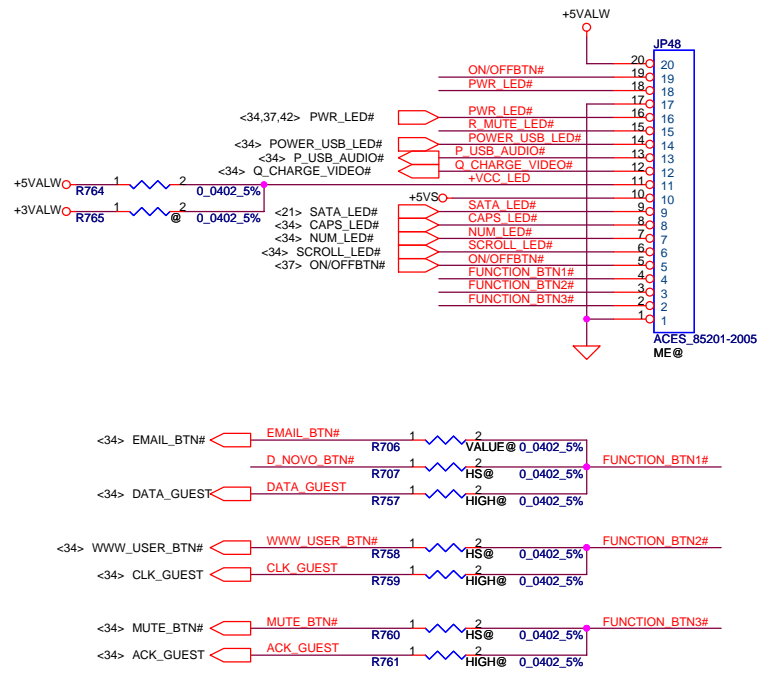
## For IFL90



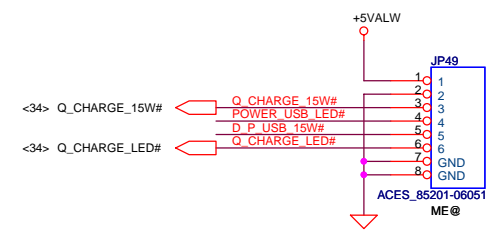
## For IFT00



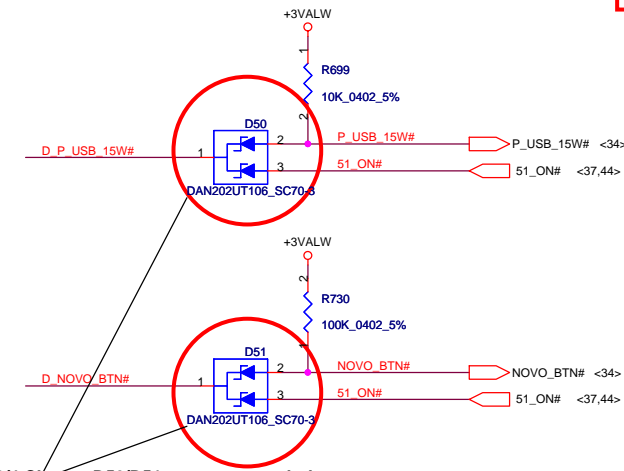
## Switch Board Conn.



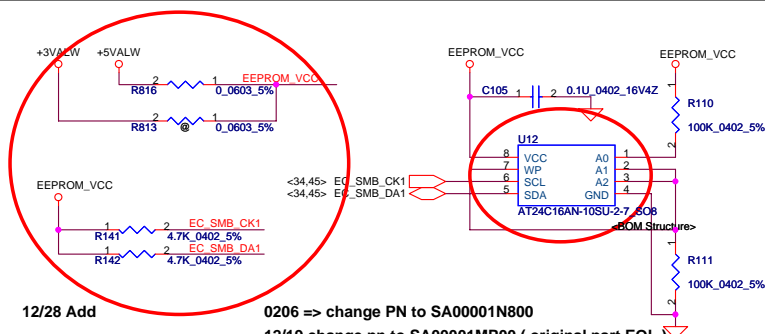
## Video Switch Board Conn.



12/4 Change D50/D51 to correct symbols



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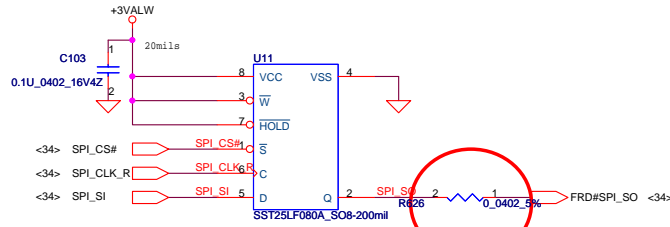
12/28 Add

0206 => change PN to SA00001N800

12/19 change pn to SA00001MP00 ( original part EOL )

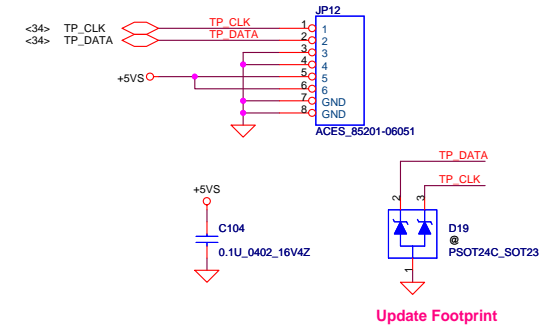
12/25 change back to SA024160140 ( Samples can not on time )

## 8M SPI ROM



12/15 change from 15 to 0 ohm\*

## To TP/B Conn.



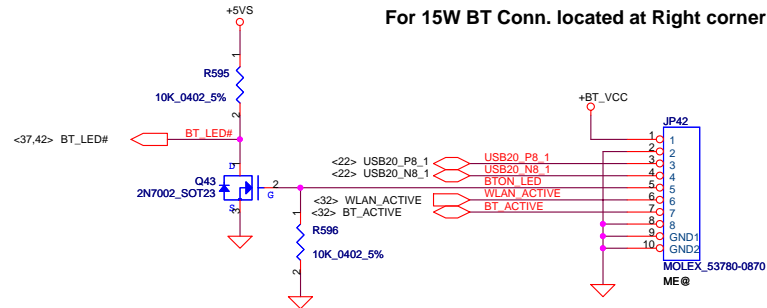
Update Footprint

## Bluetooth Conn.

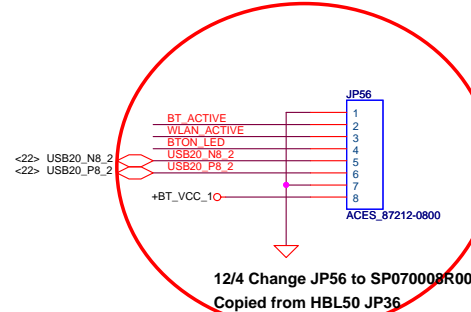
Need to check BT pin definition again!

9/20 modified this block

For 15W BT Conn. located at Right corner



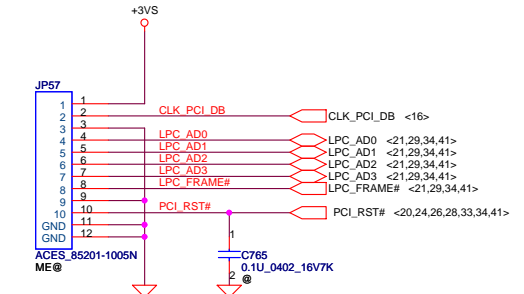
For 14W BT Conn. located at Left corner



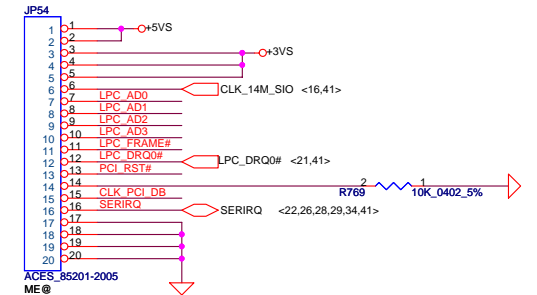
12/4 Change JP56 to SP070008R00

Copied from HBL50 JP36

## FOR LPC DEBUG PORT



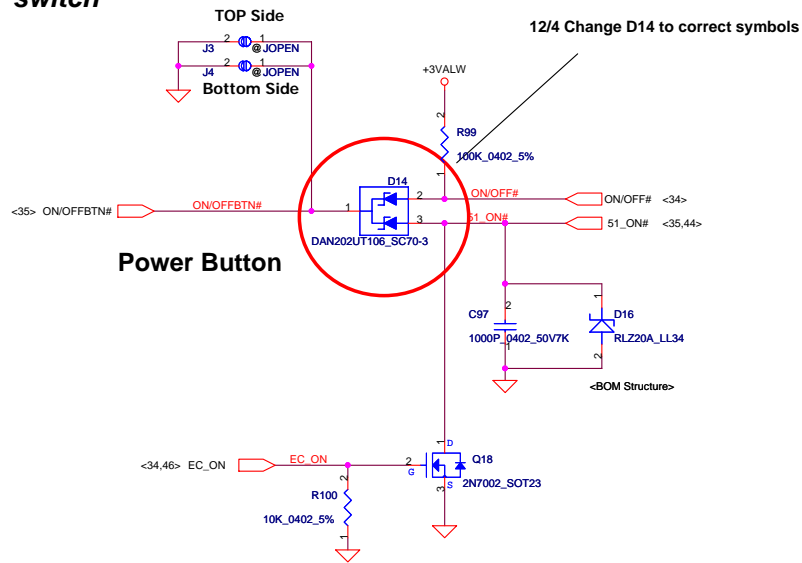
## FOR LPC SIO DEBUG PORT



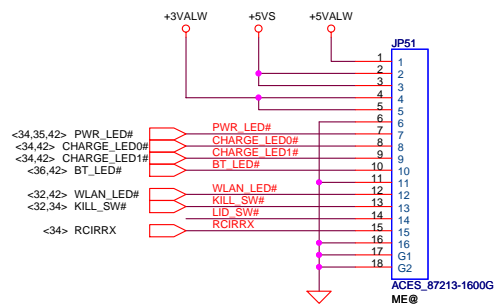
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title			
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						Size B		Document Number		Rev	
						IFTXX M/B LA-3541P Schematic					
						Date		Friday, February 09, 2007		Sheet 36 of 53	



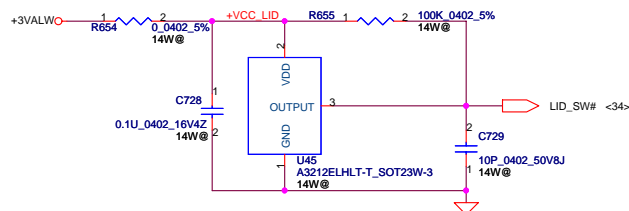
## ON/OFF switch



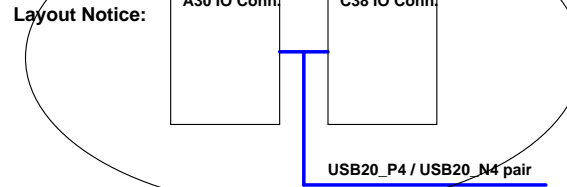
## Front LED Board



## Lid Switch

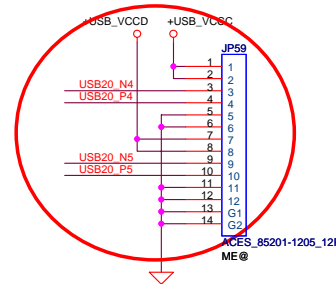


## Layout Notice:

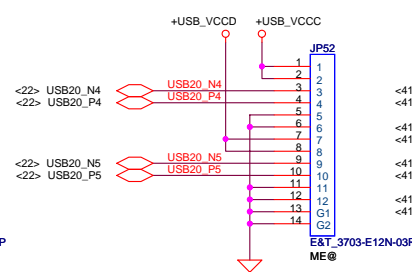


0207 Add JP59 0209 Change Symbol for GND PAD

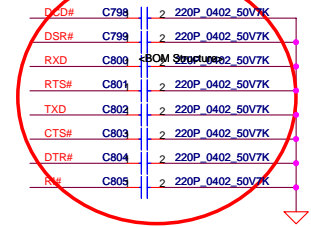
## For 15W IO Conn.



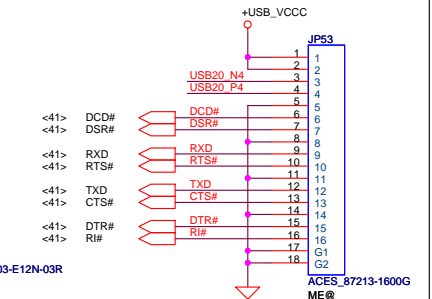
## For 14W IO Conn.



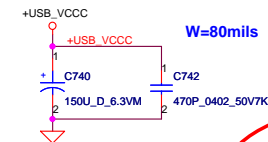
0208 Add 220pF for EMI



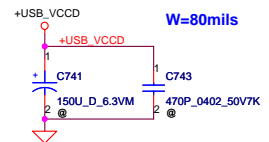
## For C38 IO Conn.



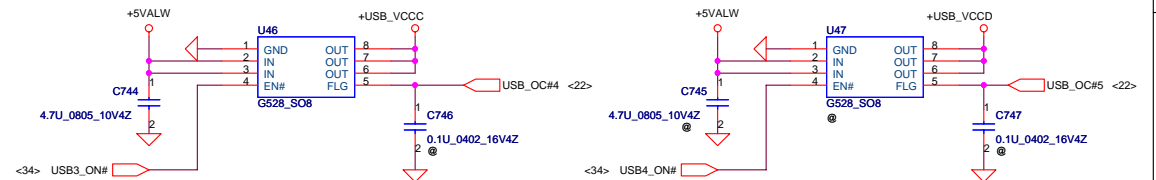
## To USB CONN. 3



## To USB CONN. 4

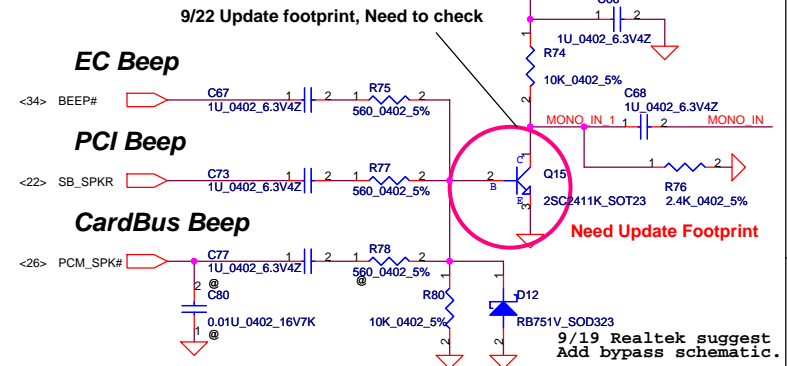
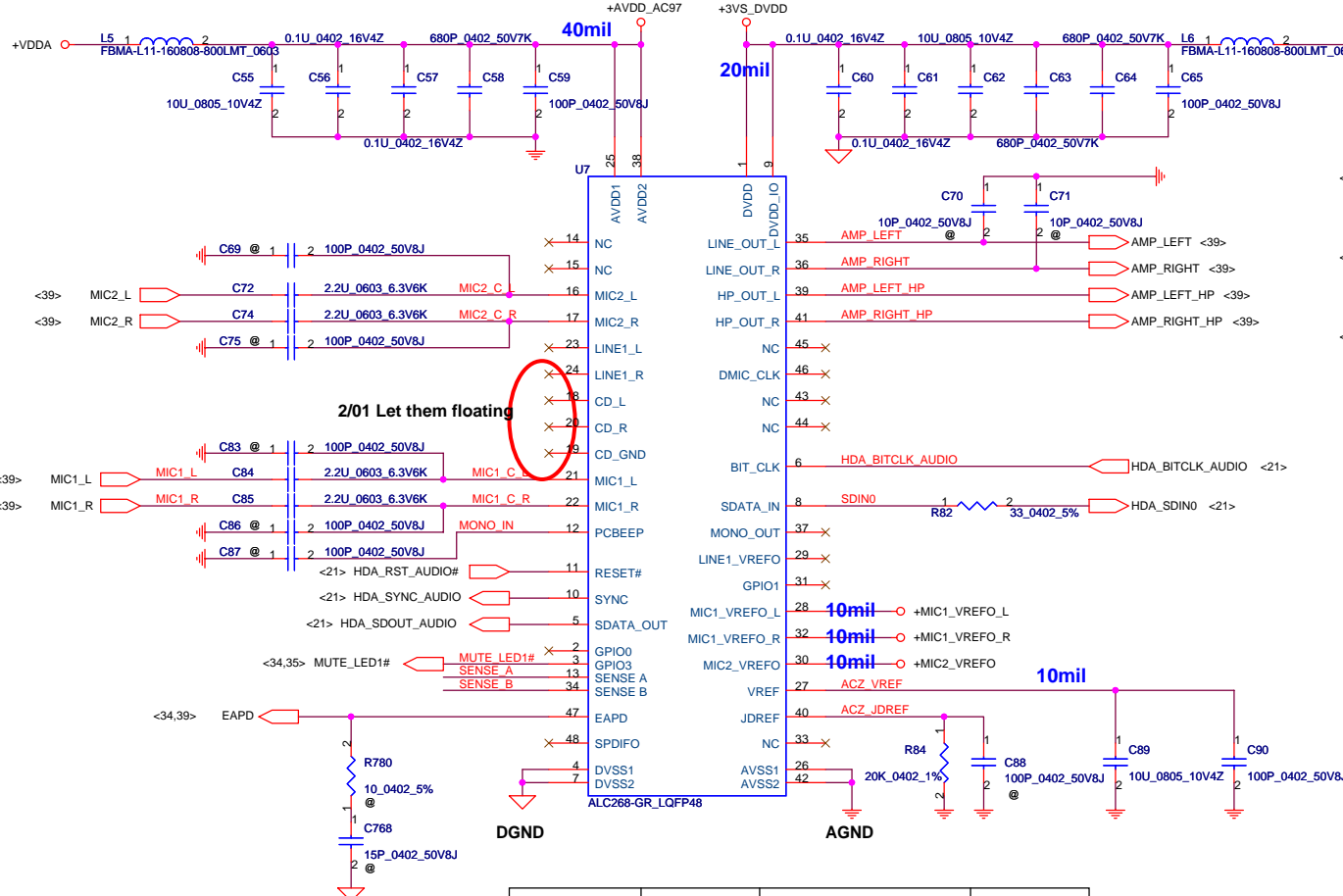


12/19 Add  
12/27 modified to A30@



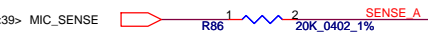
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Title			
Deciphered Date				2007/8/18				Power OK, Reset and RTC Circuit, TP			
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# HD Audio Codec

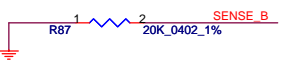


2/01 Let them floating

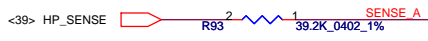
SENSE FOR Ext. Mic.



SENSE FOR Solo Int. Mic.

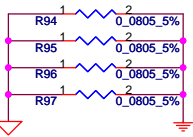


SENSE FOR HP

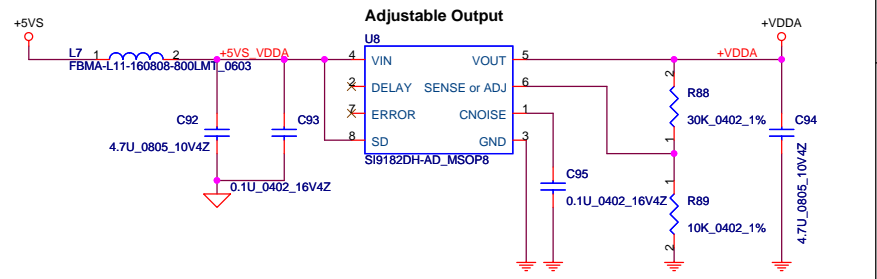


Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

Moat Bridge

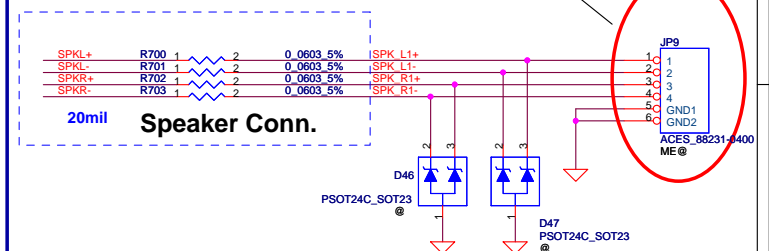
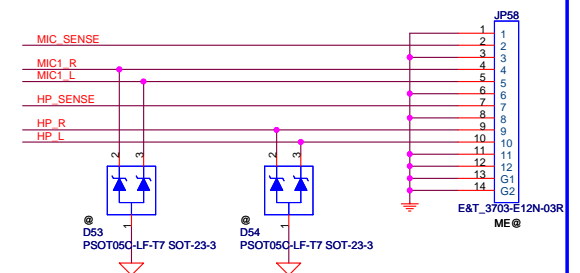
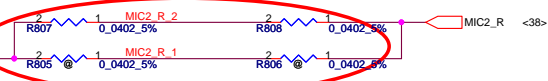
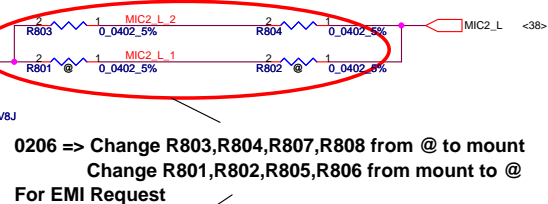
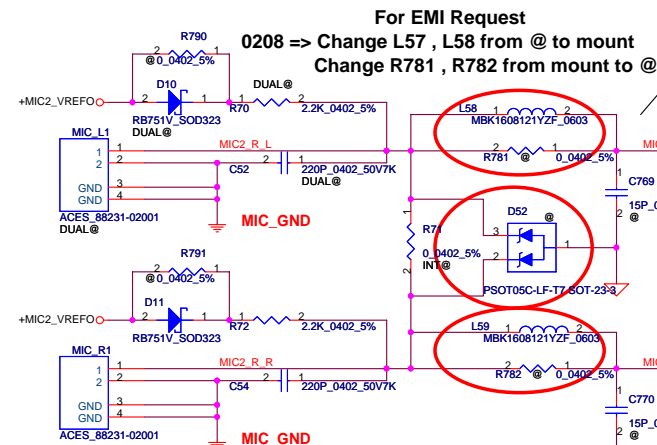
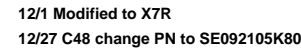
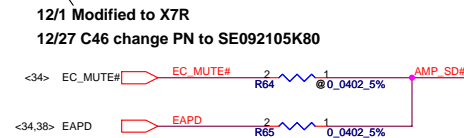
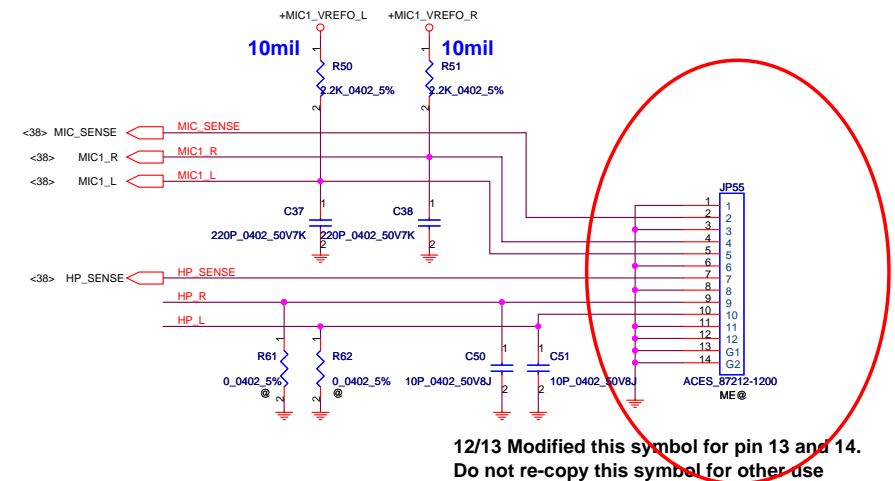
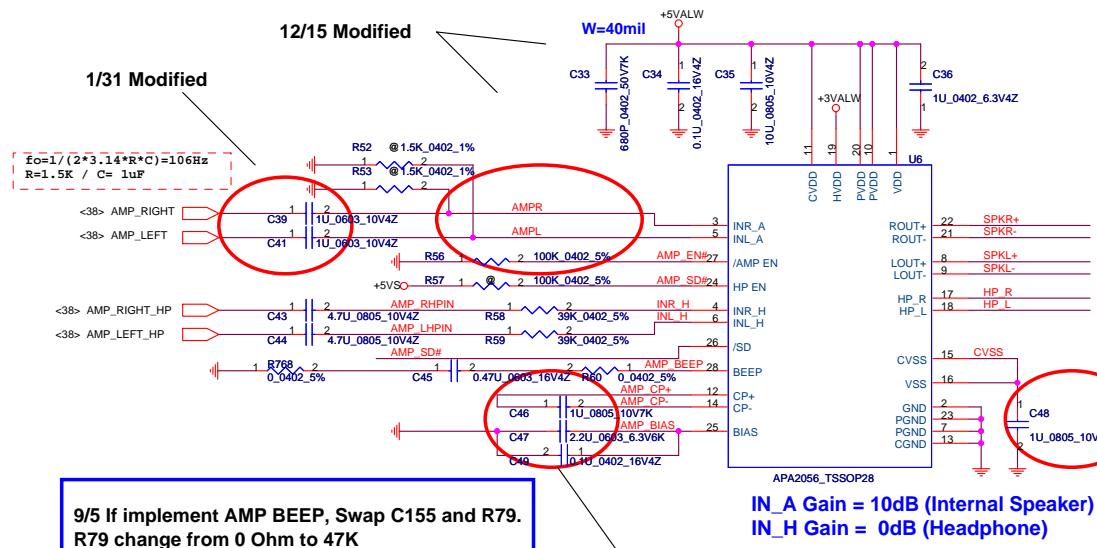


Regulator for CODEC

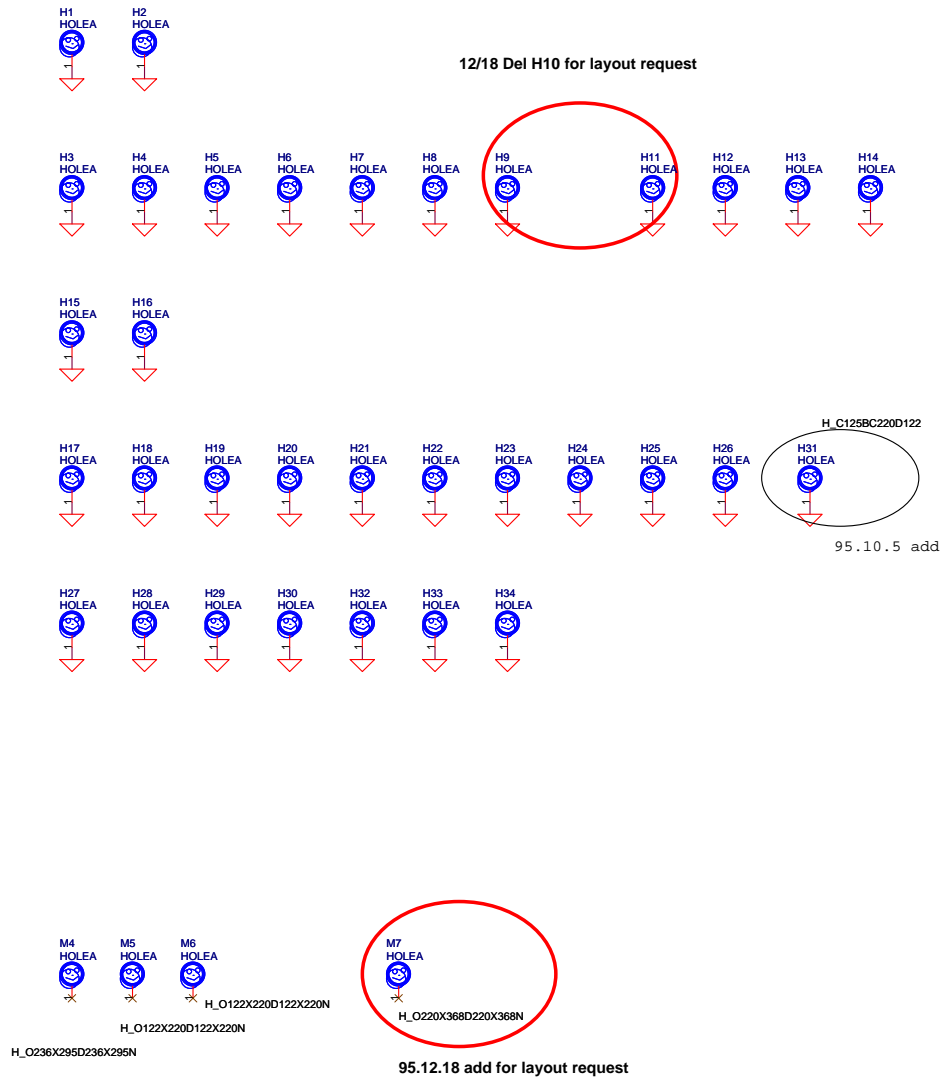


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								Custom	LA-3541P	0.1	
								Date:	Friday, February 09, 2007	Sheet 38 of 53	

## APA2056 SPK/HP Amplifier

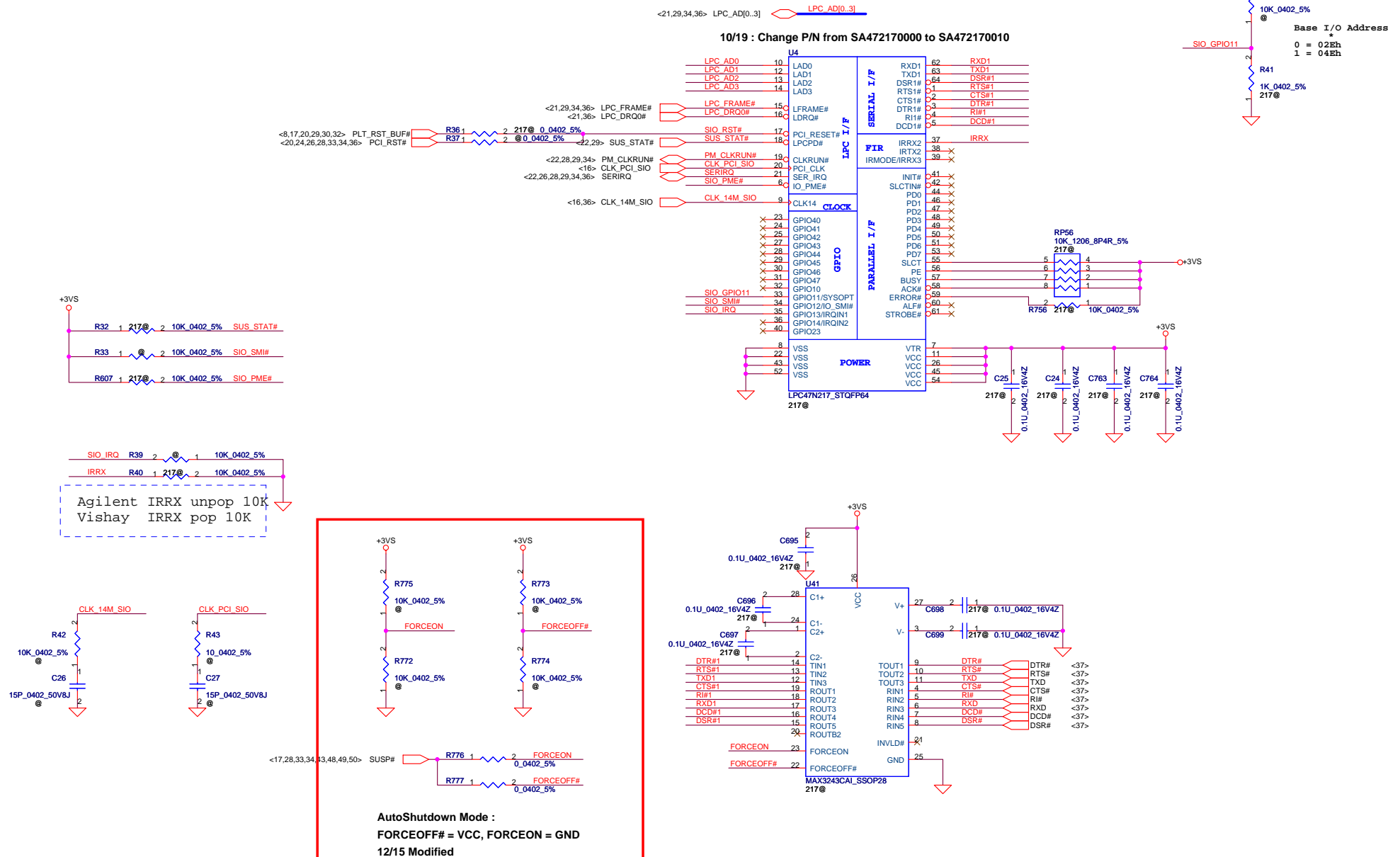


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				Custom	LA-3541P	



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Size B	Document Number			Rev		
0						
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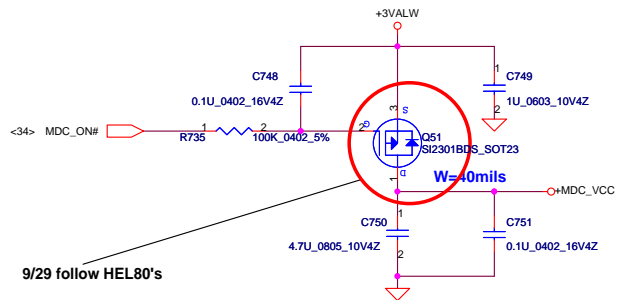
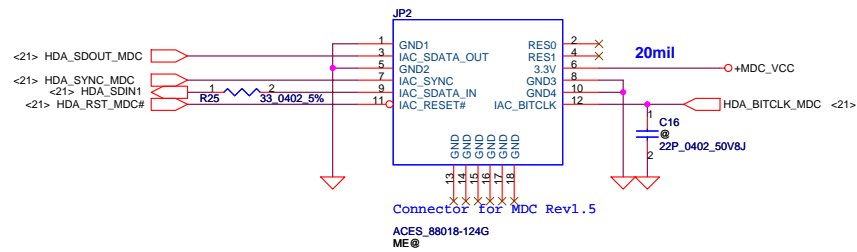
# SUPER I/O SMsC LPC47N217



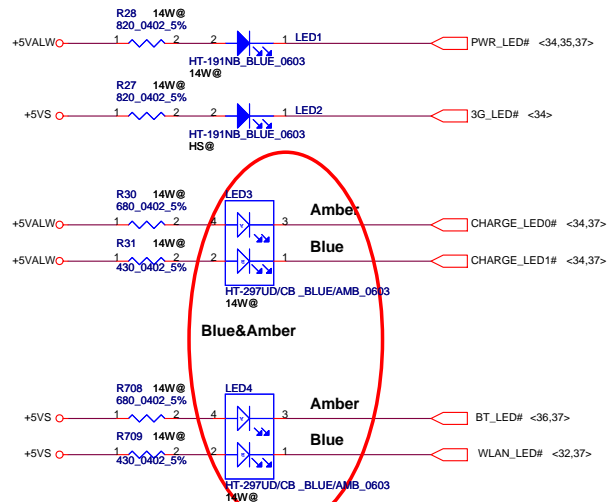
9/18 modify this page following IGT1x

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## MDC Conn.

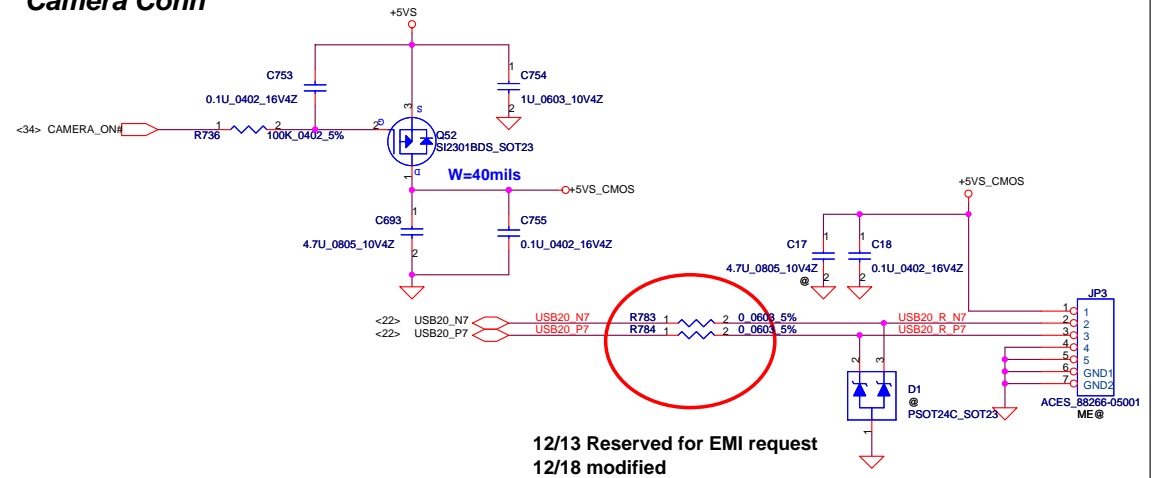


## LED



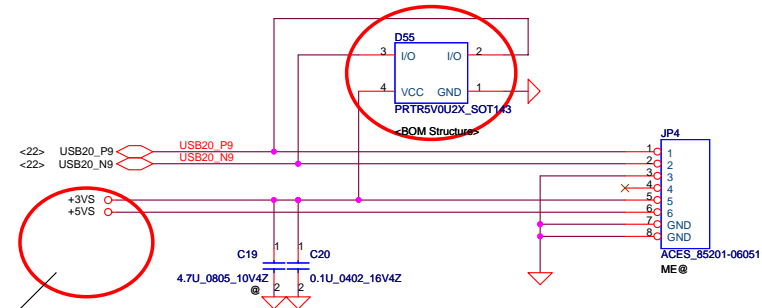
12/7 Modified LED footprint to LED\_HT-297UD-CB\_4P  
12/15 Modified to correct LED symbol!

## Camera Conn



## Finger Print board

1/05 Modified D3 to SCA00000A00 For EMI  
0208 Remove D3, Add D55 (SC300000G00)



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								2007/8/18			
Title				MDC/CIR & LED				Rev			
Size				Document Number				0			
Date:				Thursday, February 15, 2007				Sheet			
								42 of 53			

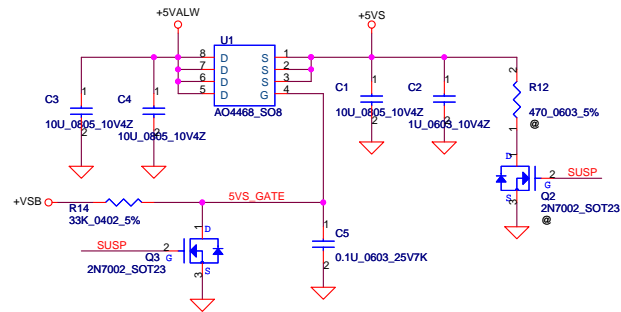
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ACES\_85201-06051  
ME@

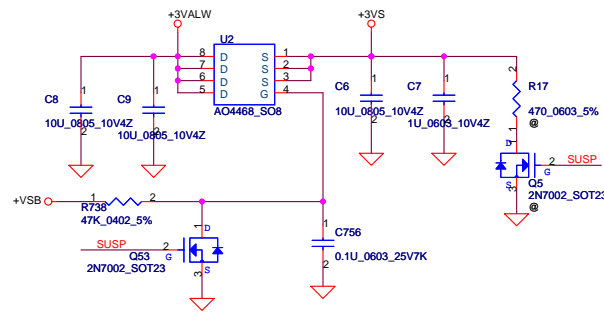


1/18 Change U3 PN from  
SB000009580 to SB000005D80

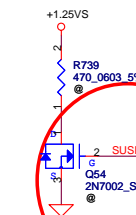
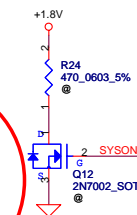
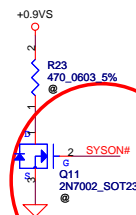
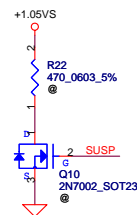
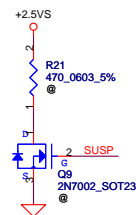
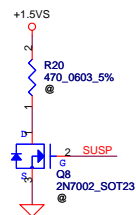
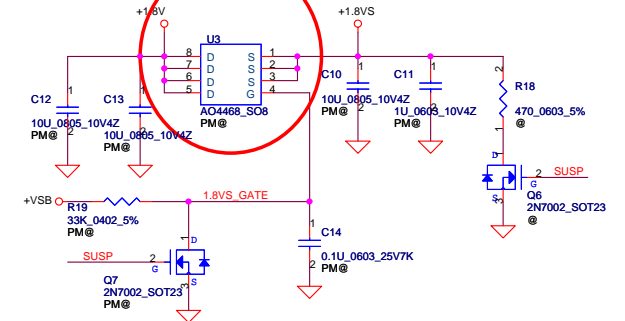
### +5VALW TO +5VS



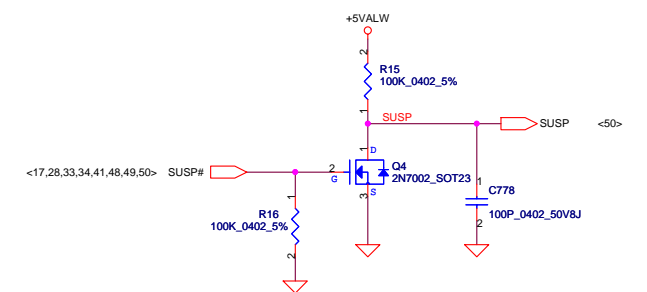
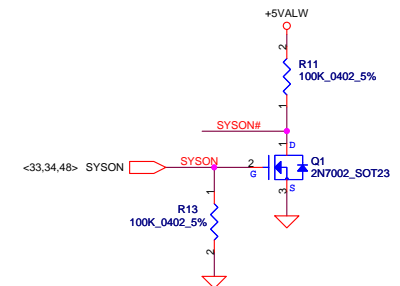
### +3VALW TO +3VS



### +1.8V to +1.8VS

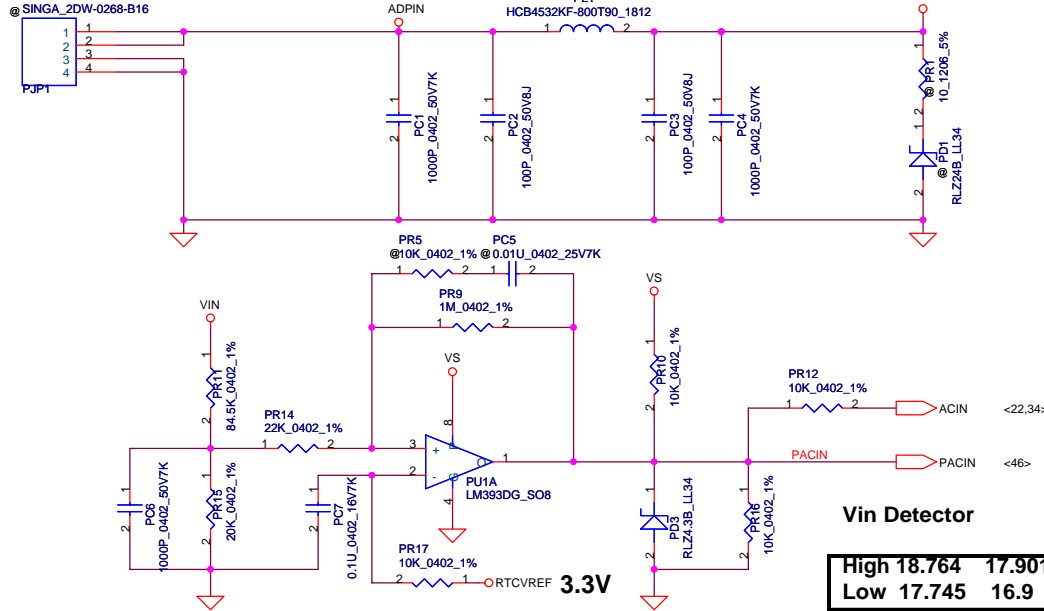


12/7 Modified



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				Size B	Document Number		Rev
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Date:		Thursday, February 08, 2007		Sheet	43	of 53	

DC301001Y00

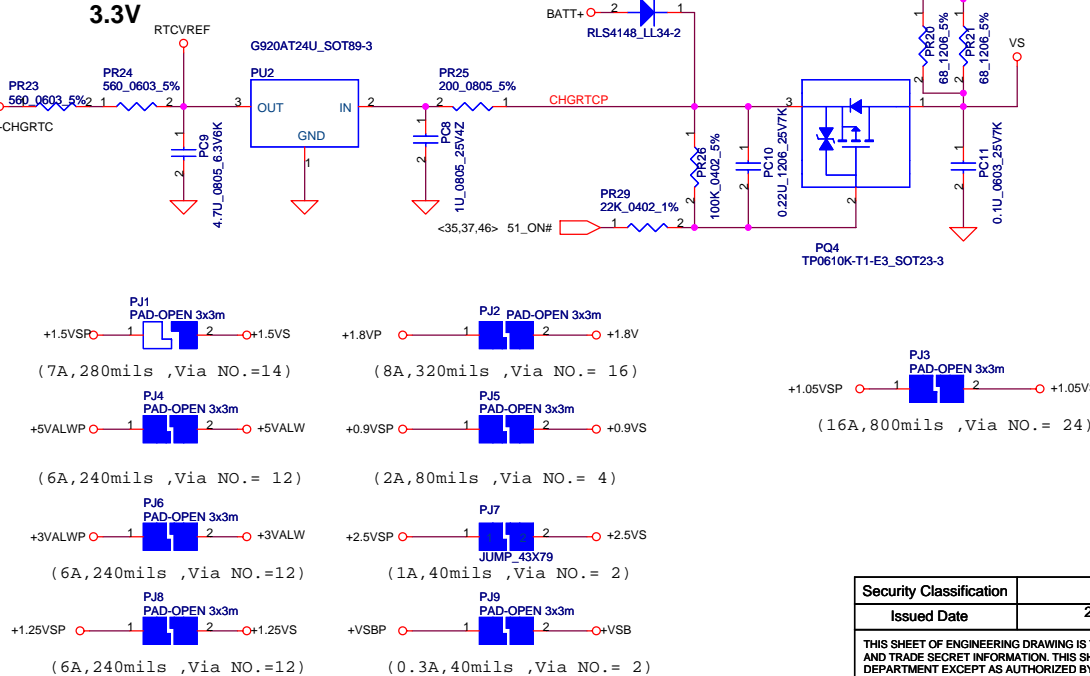
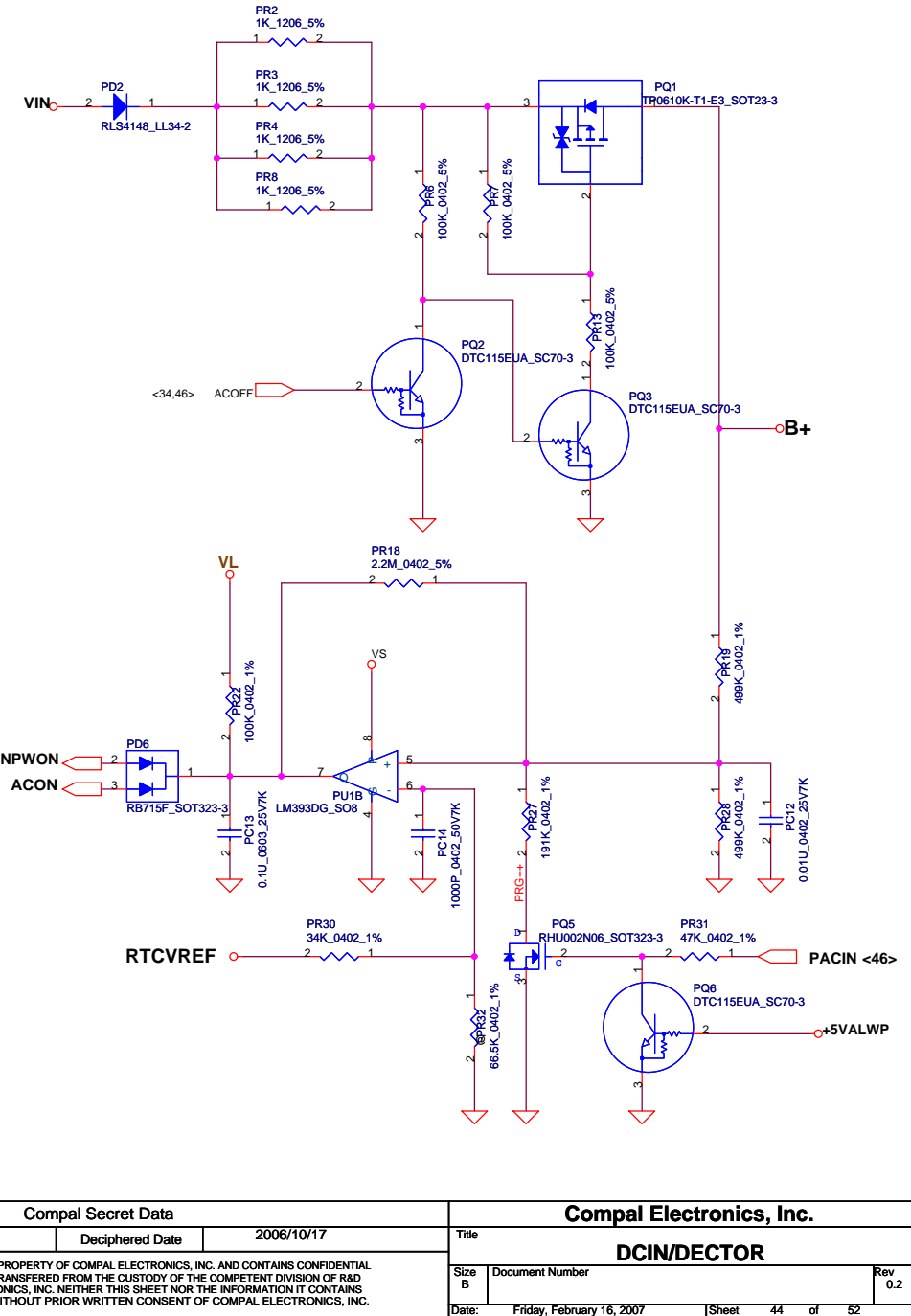


ACIN

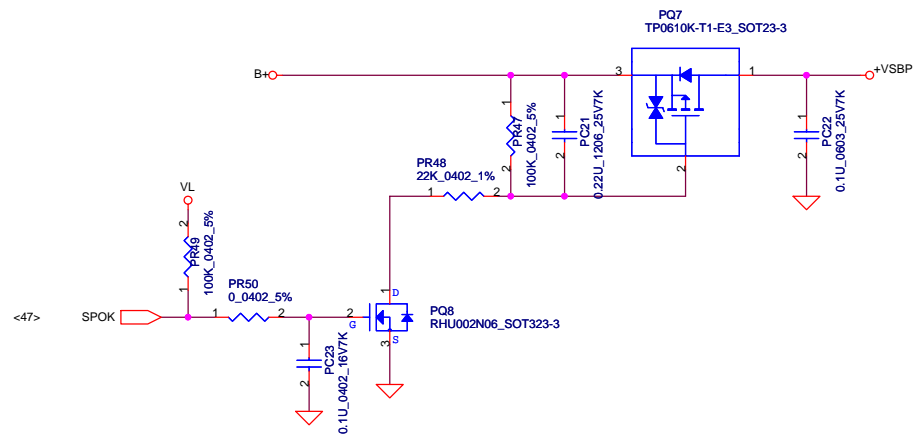
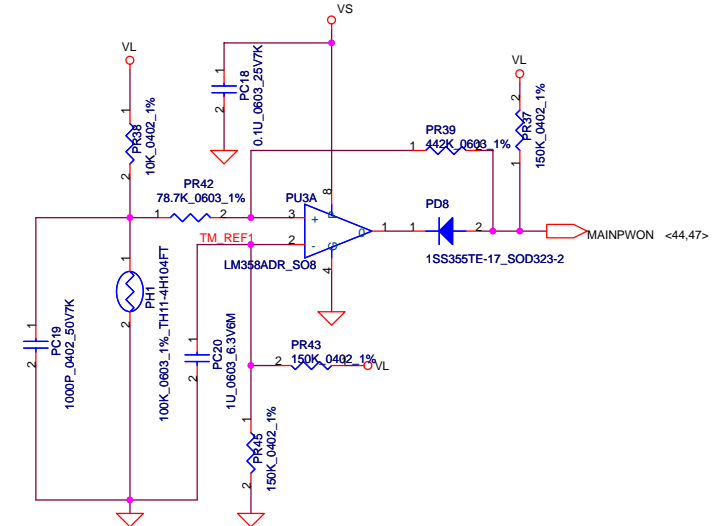
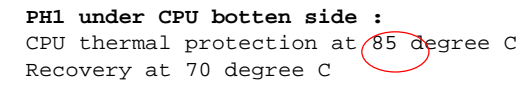
Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



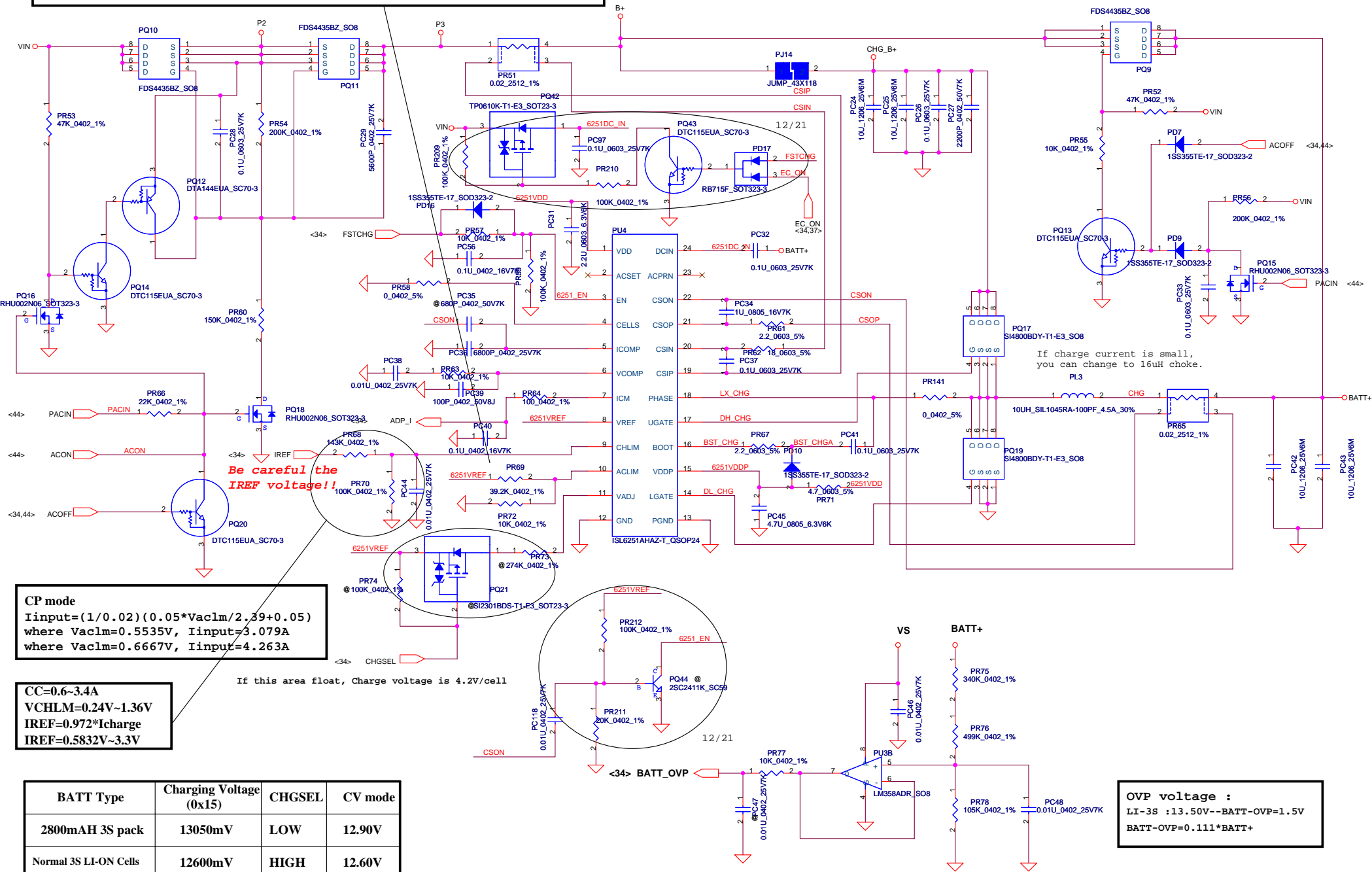
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2005/10/17				Title			
Deciphered Date				2006/10/17				DCIN/DECTOR			
Size				Document Number				Rev			
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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A  
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

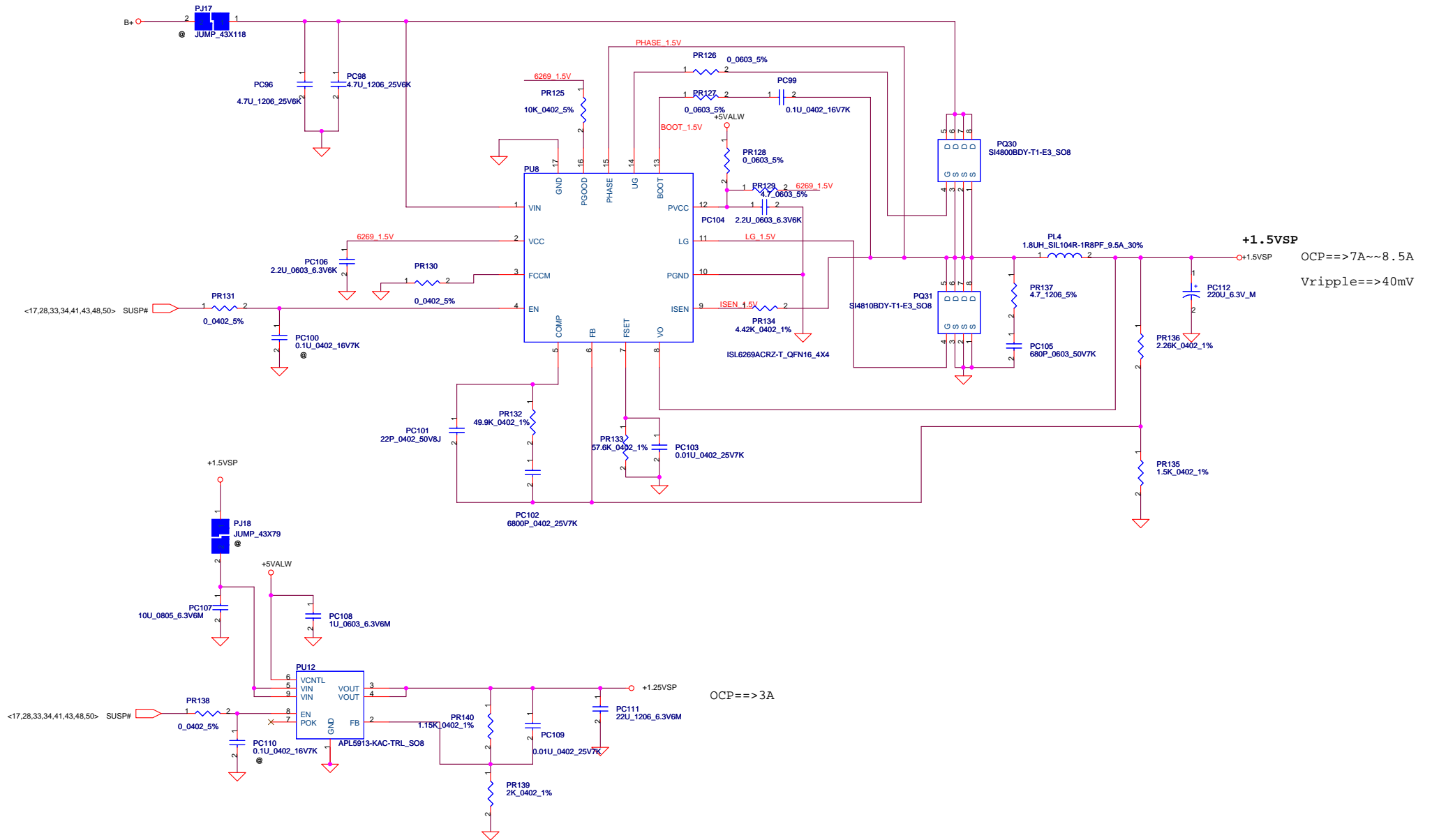
ADP\_I = 19.9\*Iadapter\*Rsense



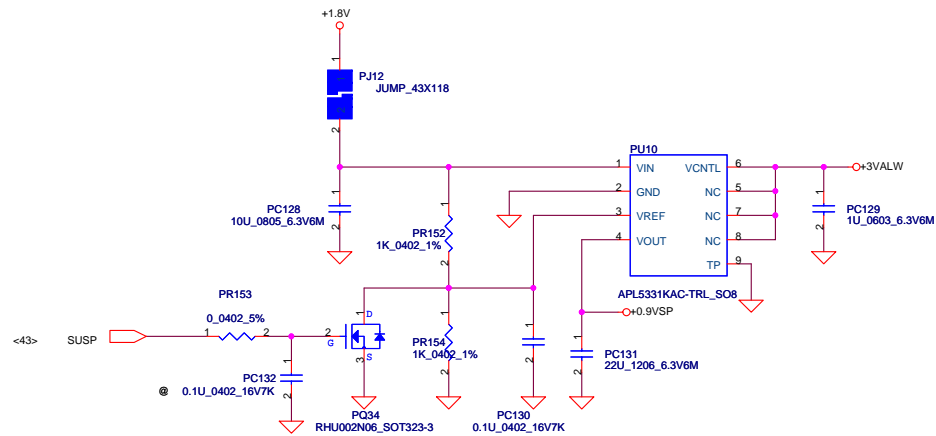
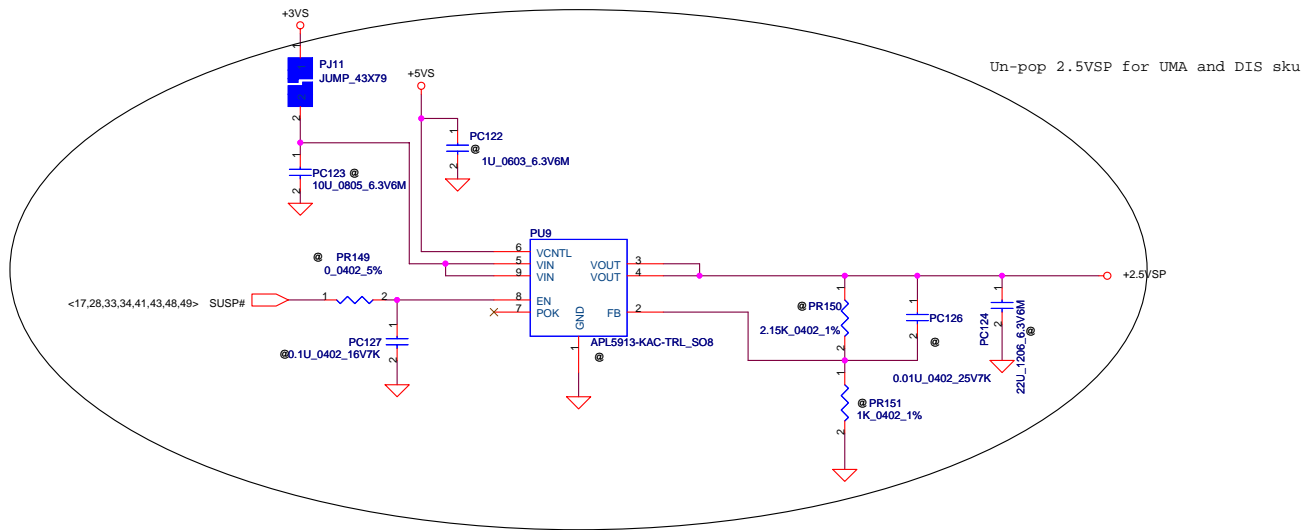




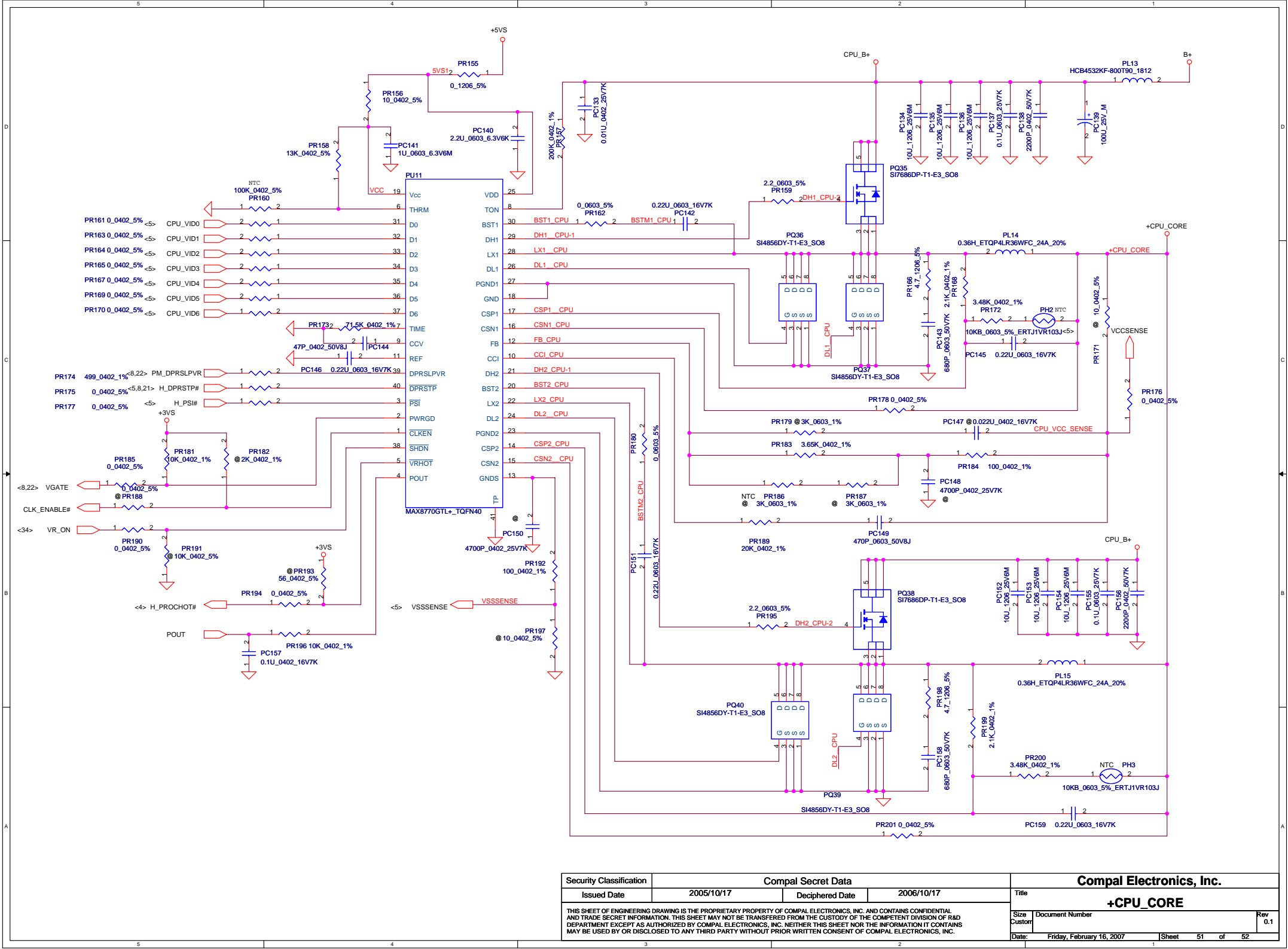




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						1.5VSP/1.25VP							
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		5	4	3	2	1
D	page	Reason for change	Modify list			
	Pre EVT P50	For H/W 0.9V sequence deamd	Delete PQ34			
		Modify Bead to Jump for costdown	PL1,PL2,PL4,PL7,PL10			
		Modify 10UH/X6S to 10UH/X5R for common source	PC53,PC57,PC96,PC116,PC134,PC135,PC136,PC152,PC153,PC154			
		Modify CH751H to RB751V for common source	PD10			
	DVT					
	95/12/28	Keep Batt_OVP to 1.5V	Change PR78 form 150K to 105K			
		Take out PC148 & PC150 form VTT tool test	Delete PC148 &PC150			
		Adjust PR183 to 39.2K for loadline	PR183			
		Modify CPU_High side form SI7840 to SI7686 for vender shortage	PQ35,PQ38			
C		Modify PosCAP to Alu CAP for cost	PC63,PC87,PC99			
		DFX footprint issue, Modify RLS4148_LLDS2 to LL34	PD2,PD4			
		Add skip mode function form skip pin of 3/5V IC	PR203			
		ADD Battery in function in page 45	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41			
		Defence charger IC leakage current in page 46	PR57,PR209,PR210,PR211,PR212,PC118,PC97,PC56,PD16,PD17,PQ42,PQ43,PQ44			
		ADD Battery in and DC-IN Bead	PL1,PL2			
		ADD 100PF in SPOK PIN for noise but unpop	PC30			
		ADD CPU high side gate resister 2.2 OHM for EMI demand	PR159,PR195			
		Change PR137 to L/F	PR137			
		Change PR95 form 6.81K to 6.49K for power loss	PR95			
B	96/01/03	Disable battery in function, EC control	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41			
		Modify 0.01U_0402 to 1000P_0402	PC1,PC4			
		Remove PR1 & PD1 for cost	PR1,PD1			
		Modify AO4407 to FDS4435 for UMA cost	PQ10,PQ11,PQ9			
		Modify RB751V to 1SS355 for cost	PD12,PD13,PD14,PD15,PD10			
		Remove 2.5VSP function for UMA	PR149,PR150,PR151,PC122,PC123,PC124,PC126,PC127,PU9			
		Change 1.05VSP High/Low side MOS for cost	PQ26,PQ27			
		Change 0.9UH to 1.8uH for 1.05vsp cost	PL8			
		Change PC72 330U/R9 to 330U/R15. and del PC88	PC72,PC88			
		Add PR207 280K_0402 and delete PR202	PR207,PR202			
A		Modify PC139 for 100uH at 3000hurs	PC139			
		Modify charge Low side gate to SI4800BDY	PQ19			
		5	4	3	2	1

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	5	4	3	2	1
	page	Reason for change	Modify list		
96/01/03 DVT		Disable battery in function, EC control	PR204,PR205,PR206,PR207,PR208,PC51,PC52,PQ41		
		Modify 0.01U_0402 to 1000P_0402 for common design	PC1,PC4		
		Remove PR1 & PD1 for common design	PR1,PD1		
		Modify AO4407 to FDS4435 for UMA	PQ10,PQ11,PQ9		
		Modify RB751V to 1SS355 for common design	PD12,PD13,PD14,PD15,PD10		
		Remove 2.5VSP function for UMA sku	PR149,PR150,PR151,PC122,PC123,PC124,PC126,PU9		
		Change 1.05VSP High/Low side MOS for rating	PQ26(SI4800),PQ27(Si4810)		
		Change 0.9UH to 1.8uH for 1.05vsp rating	PL8		
		Change PC72 form 330U/R9 to 330U/R15. and del PC88 for rating	PC72,PC88		
		Add PR107 280K_0402 and delete PR202 for 1.05VSP OCP	PR107,PR202		
		Modify PC75 form 4700P to 3300P for 1.05VSP OCP	PC75		
		Modify PC139 for 100uH at 3000hurs	PC139		
96/01/19 DVT-2		Modify charge Low MOS gate to SI4800BDY	PQ19		
		Disable CC-CV overshoot function , need verify it.	PQ44		
		0.9V sequence for H/W deamd	Add PQ34		
96/01/19 PVT		Change CPU low side mos to SI4856	PQ36,PQ37,PQ39,PQ40		
		Chage 1.5V/1.25V dual to single and LDO portion	DEL PR141,PR143,PR144,PR145,PR146,PR148,PC110,PC113,PC114,PC115,PC116,PC117,PC120,PC121,PL11,PL12, PQ32,PQ33,PD14,PD15		
			ADD PR125,PR126,PR136,PU12,PL4		
			Modify PR128,PR129,PR130,PR131,PR132,PR133,PR134,PR135,PR136,PR137,PR138,PR139,PR140		
			PC96,PC98,PC99,PC101,PC102,PC103,PC104,PC105,PC106,PC107,PC108,PC109,PC111,PC112		
			PU8		
		Combine PU5 LM358 and PU3 LM393	Del PU5,ADD PD8		
		Change PD5 form RB751 to RLS4148 for cost	PD5		
		Change 0.1U_0603 to 0.1U_0402 for cost	PC49,PC50,PC74,PC84,PC81		
		Remove PC147 for cost	PC147		
		Change PC128 form 10U_1206 to 10U_0805 for cost	PC128		
96/02/16 PVT		Modify CPU OTP 85 degree C to 89 degree C for thermal request	PR42_78.7K, PR38_10K		